# FEATURES

- 8.6V to 14.7V Input Supply Voltage Range for TV
- 4.3V to 6V Input Supply Voltage Range for MNT
- Fully I²C Interface Control
- 1-bit Selectable Switching Frequency for AVDD, VBK1, VGH, VGL (500kHz/750kHz)
- Optional Internal or External MOSFET Drive Boost Regulator for AVDD
  - 13.5V to 19.8V Output Voltage Range
- Synchronous Buck Regulator for VBK1
  - 1.8V to 3.35V Output Voltage Range
- High-Current Programmable Amplifier for HAVDD
  - 7-Bit Resolution
  - ±200mA Output Short-Circuit Current
- Optional Inverting Regulator Converter or Charge Pump Regulator for VGL
  - –3V to –18V Output Voltage Range
  - Temperature-compensated Output
- The Negative Linear Regulator for VSS1
  - –3V to –16V Output Voltage Range
  - Sourcing and Sinking Capacity
- Optional Boost Regulator or Change Pump Regulator for VGH
  - 20V to 45V Output Voltage
  - Temperature-compensated Output
- 1-Channel Programmable Amplifier for VCOM1
  - 7 Bit Resolution
  - ±400mA Short-Circuit Current
- 1-Channel Programmable VCOM2 DAC
  - 7 Bit Resolution
- 14-Channel Programmable Gamma Amplifiers
  - 10 Bit Resolution
  - ±100mA Short-Circuit Current
- Protection
  - UVP, SCP, OTP
- Slave Address: 0100 000 R/W (PMIC)
  1110 100 R/W (VCOM1)
- WQFN 6.5x4.5-46 Package
- WQFN 6x6-48L Package

# GENERAL DESCRIPTION

The iML1942 is a highly integrated power management IC for TFT LCD panels. It features fully I²C interface to program various parameters.

The device consists of one current mode boost regulator for AVDD, one synchronous buck converter for VBK1. An optional inverting converter or negative charge pump regulator for VGL with temperature-compensated output, a negative linear regulator for VSS1, an optional boost regulator or charge pump regulator for VGH with temperature-compensated output, a programmable amplifier for VCOM1, a programmable DAC for VOCM2 and 14-channel programmable Gamma amplifiers.

The iML1942 device includes various protection features such as input under-voltage lockout (UVLO) and over temperature shutdown (OTP). The outputs include under voltage protection (UVP), and short circuit protection (SCP).

The iML1942 is available in a WQFN 46 pin 6.5 mm X 4.5 mm with a bottom side exposed thermal pad to provide optimal heat dissipation. The device is rated to operate from –40 to +85°C temperature range.

# APPLICATIONS

- Monitor Panel
- TV Panel

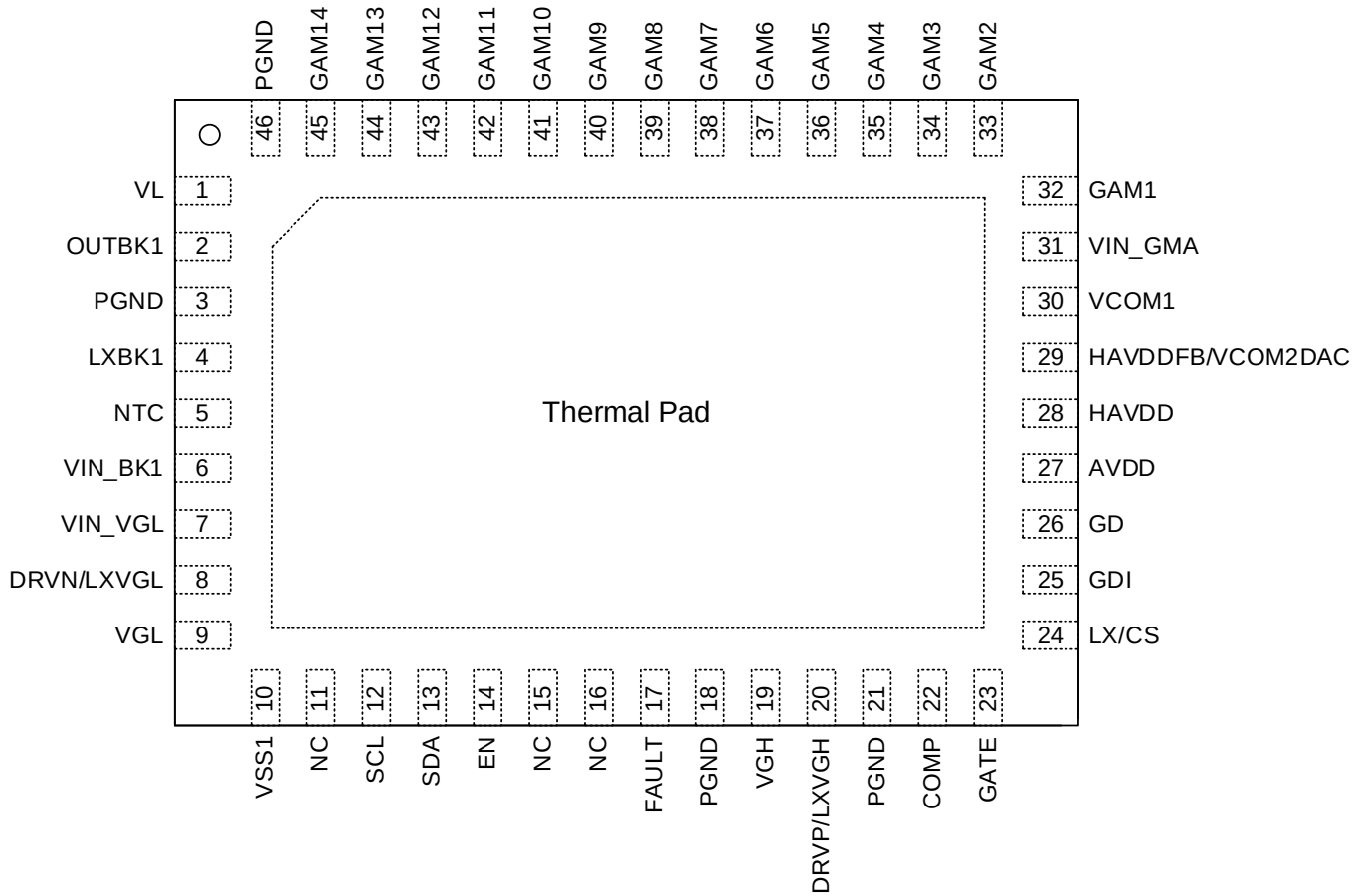
# ORDERING INFORMATION

| DEVICE TYPE | PART NUMBER | PACKAGE | PACKING | TEMP. RANGE | MARKING | MARKING DESCRIPTION |
|---|---|---|---|---|---|---|
| iML1942 | iML1942UM-TR | WQFN 6.5x4.5-46L | Tape and Reel | –40 °C to +85 °C | i1942 XXXXXXXX | i1942: Part Name XXXXXXXX: Tracking number |
| iML1942 | iML1942KM-TR | WQFN 6x6-48L | Tape and Reel | –40 °C to +85 °C | i1942 XXXXXXXX | i1942: Part Name XXXXXXXX: Tracking number |

Note 1: All CHIPONE products are lead free and halogen free.

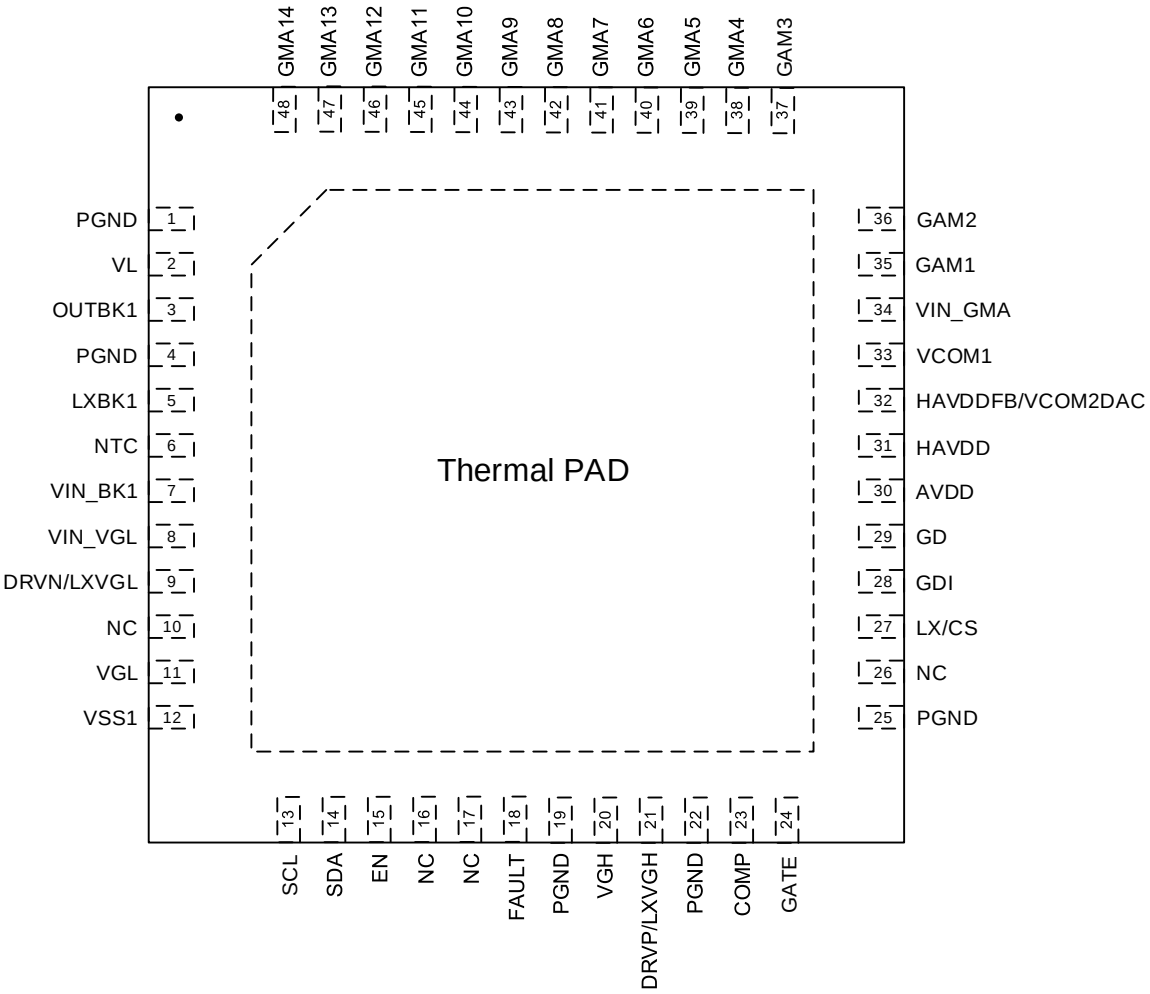
# PIN CONFIGURATION

WQFN6.5*4.5-46L




**TOP View**

QFN6*6-48L




**TOP View**

# TYPICAL APPLICATION

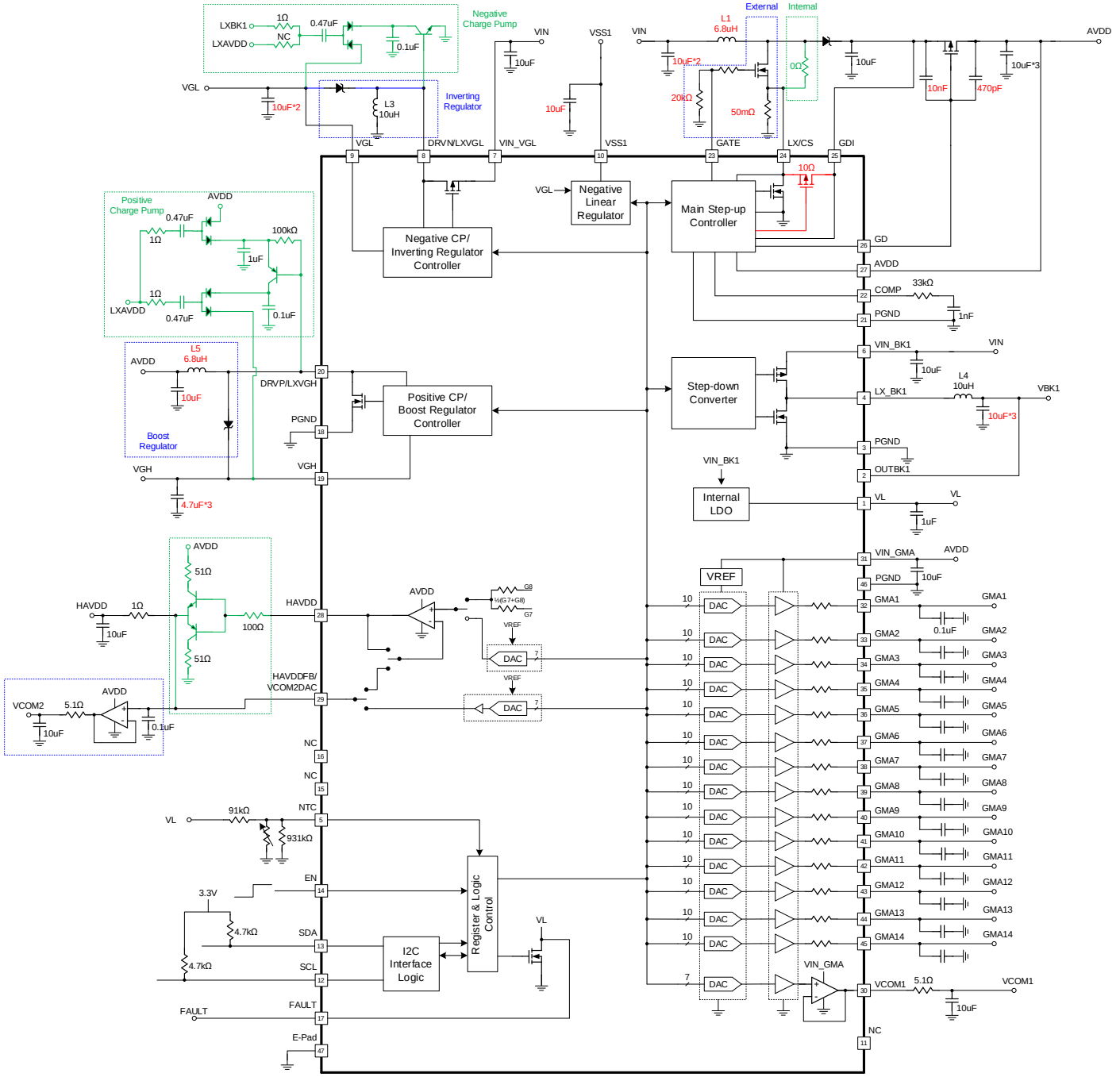



Figure 1. The iML1942 application circuit

# PIN DESCRIPTION

| PIN No. QFN6.5*4.5-48L | PIN No. QFN6*6-48L | Name | I/O | Description |
|---|---|---|---|---|
| 1 | 2 | VL | O | Internal regulator output. Connect this pin with a decoupling capacitor. |
| 2 | 3 | OUTBK1 | I | Feedback voltage input for VBK1 step-down regulator. |
| 3,18,21,46 | 1,4,19,22,25 | PGND | P | Power ground pin. |
| 4 | 5 | LX_BK1 | I/O | Switching node of VBK1 step-down regulator. |
| 5 | 6 | NTC | I | Temperature compensation input pin. Connect NTC thermistor and resistors to this pin to control the slope of VGH/VGL voltage for temperature compensation. |
| 6 | 7 | VIN_BK1 | P | Power input for VBK1 step-down regulator. |
| 7 | 8 | VIN_VGL | P | Power input for VGL inverting regulator. |
| 8 | 9 | DRVN/LXVGL | I/O | DRVN: (VGL charge-pump mode) negative linear regulator base drive.<br>LXVGL: (VGL inverting mode) switching node of the inverting regulator. |
| 9 | 11 | VGL | I | (VGL charge-pump mode) VGL regulator output sense.<br>(VGL inverting mode) VGL inverting regulator output sense. |
| 10 | 12 | VSS1 | O | VSS1 negative linear regulator output. |
| 11,15,16 | 10,16,17,26 | NC | -- | No connection. Need to connect to PGND. |
| 12 | 13 | SCL | I | Clock input pin for the $I^2C$ serial interface. |
| 13 | 14 | SDA | I/O | Date input pin for the $I^2C$ serial interface. |
| 14 | 15 | EN | I/O | @31h, bit7=0, Enable pin of the AVDD, VGH, HAVDD, VCOM1, VCOM2DAC and GammaX. Enable pin must be connect high signal. 400kohm pull down resistor connect from this pin to ground.<br>@31h, bit7=1, XON pin for the shutdown reset function output and open drain voltage detector output. |
| 17 | 18 | FAULT | I/O | FAULT signal input/output pin. The FAULT pin is open drain output with internal pull-up resistor. The output High/Low depended on protection functions. It also can be connected the open drain circuit to control IC operations.<br>(1) Output channel UVP/SCP except VBK1 channel:<br>FAULT_O pin is Low active and all output channel shutdown except VBK1.<br>(2) VBK1 UVP/SCP:<br>FAULT_O pin is Low active and all output channel shutdown.<br>(3) External signal:<br>FAULT_I pin is Low active and all output channel shutdown except VBK1. |
| 19 | 20 | VGH | I | (VGH charge-pump mode) VGH regulator output sense.<br>(VGH boost mode) VGH step-up regulator output sense. |
| 20 | 21 | DRVP/LXVGH | I/O | DRVP: (VGH charge-pump mode) positive linear regulator base drive.<br>LXVGH: (VGH boost mode) switching node of the step-up regulator. |
| 22 | 23 | COMP | I/O | Compensation pin for AVDD step-up regulator. Connect a series RC from COMP to PGND. |

| | | | | |
|---|---|---|---|---|
| 23 | 24 | GATE | O | AVDD step-up regulator external switch drive output. This pin is used to drive external NMOS of AVDD regulator. |
| 24 | 27 | LX/CS | I/O | LX: (Internal mode) switching node of AVDD step-up regulator.<br>CS: (External mode) Current sense for external NMOS of AVDD step-up regulator. |
| 25 | 28 | GDI | I | External P-MOSFET source input to IC for AVDD (isolation switch). |
| 26 | 29 | GD | O | AVDD regulator isolated switch driver output. |
| 27 | 30 | AVDD | I | AVDD step-up regulator output sense. |
| 28 | 31 | HAVDD | O | HAVDD amplifier output. |
| 29 | 32 | HAVDDFB/<br>VCOM2DAC | I/O | HAVDDFB: Negative input of the HAVDD amplifier.<br>VCOM2DAC: VCOM2 DAC output. |
| 30 | 33 | VCOM1 | O | VCOM1 amplifier output. |
| 31 | 34 | VIN_GMA | P | Power input for GMAx and VCOM1 OP. |
| 32 | 35 | GMA1 | O | Gamma reference output 1. |
| 33 | 36 | GMA2 | O | Gamma reference output 2. |
| 34 | 37 | GMA3 | O | Gamma reference output 3. |
| 35 | 38 | GMA4 | O | Gamma reference output 4. |
| 36 | 39 | GMA5 | O | Gamma reference output 5. |
| 37 | 40 | GMA6 | O | Gamma reference output 6. |
| 38 | 41 | GMA7 | O | Gamma reference output 7. |
| 39 | 42 | GMA8 | O | Gamma reference output 8. |
| 40 | 43 | GMA9 | O | Gamma reference output 9. |
| 41 | 44 | GMA10 | O | Gamma reference output 10. |
| 42 | 45 | GMA11 | O | Gamma reference output 11. |
| 43 | 46 | GMA12 | O | Gamma reference output 12. |
| 44 | 47 | GMA13 | O | Gamma reference output 13. |
| 45 | 48 | GMA14 | O | Gamma reference output 14. |
| - | | EP | - | Exposed Pad. Connect it to ground with copper plane. |

# Power Sequence for PMIC

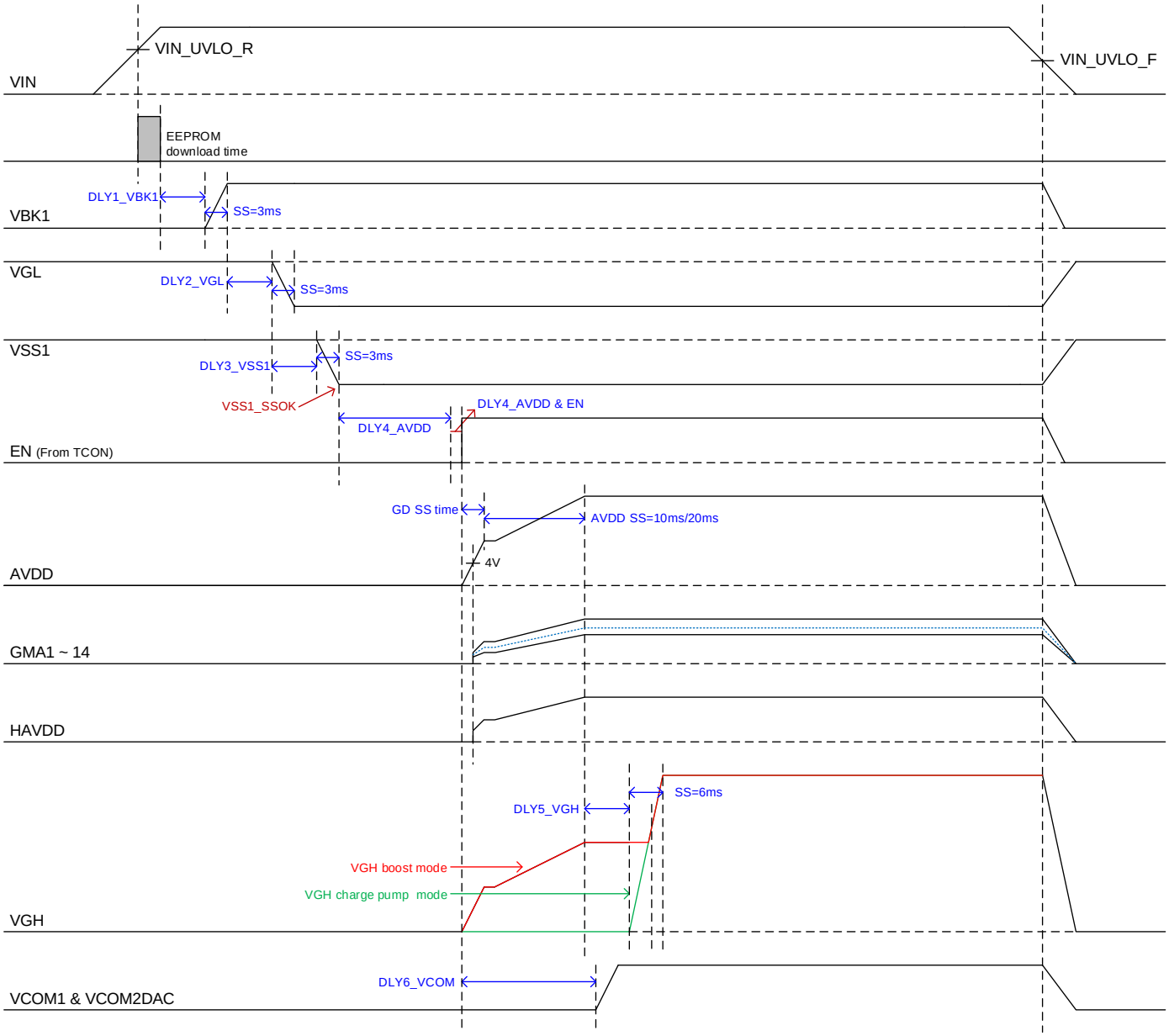



Figure 2. The iML1942 power sequence for PMIC (VGL_PUMP_SOURCE bit=0)

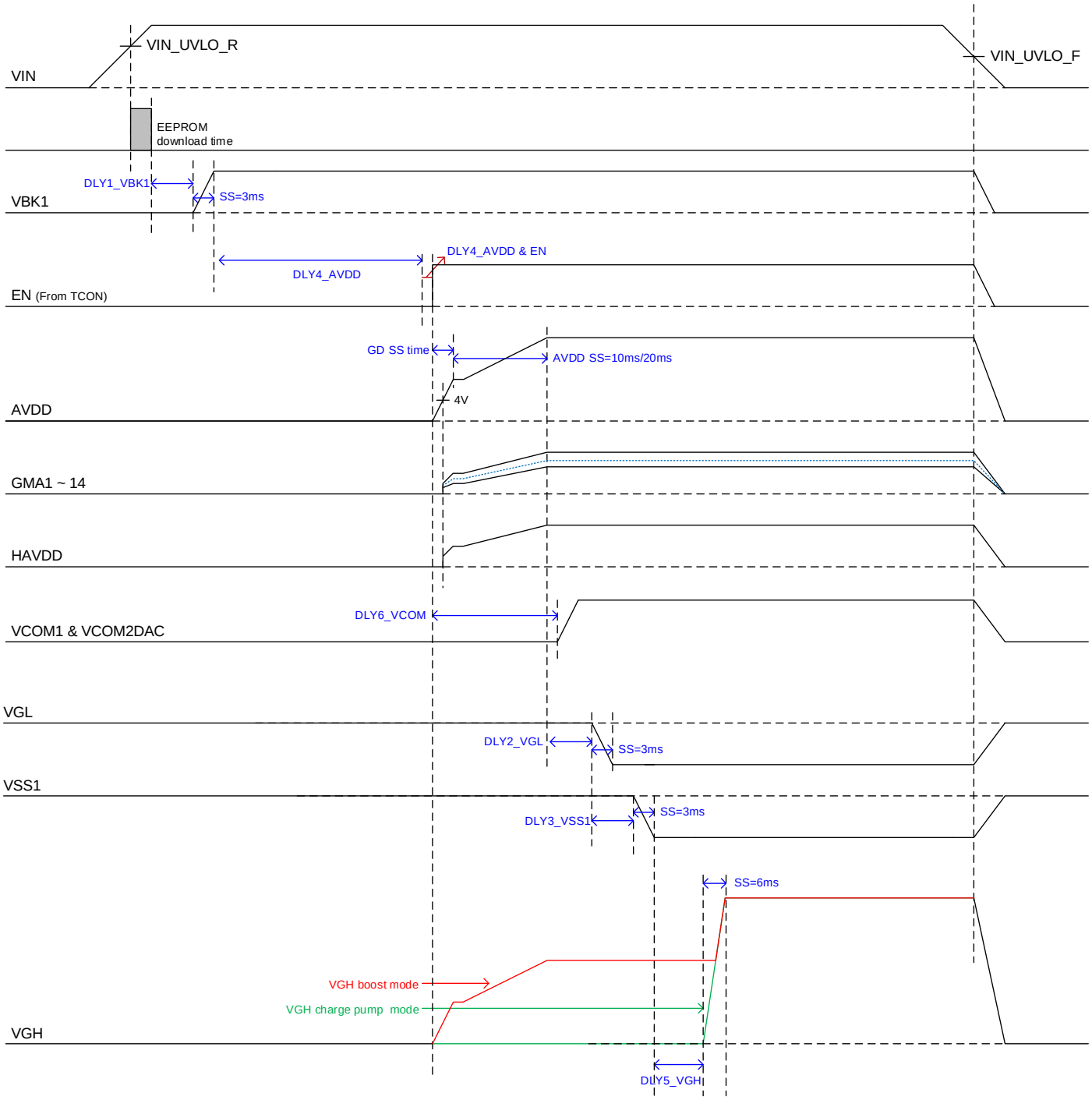



Figure 3. The iML1942 power sequence for PMIC (VGL_PUMP_SOURCE bit=1)

# ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| VIN_BK1, VIN_VGL to PGND | $V_{IN1}$ | -0.3 to +16.5 | V |
| EN to PGND | $V_{IN2}$ | -0.3 to (VIN_BK1-0.3) | V |
| COMP, NTC, SCL, SDA, FAULT to PGND | $V_{IN3}$ | -0.3 to +6.0 | V |
| VIN_GMA to GND | $V_{IN4}$ | -0.3 to +23 | V |
| GDI, GD, AVDD to PGND | $V_{H1}$ | -0.3 to +23 | V |
| HAVDD, HAVDDFB/VCOM2DAC to PGND | $V_{H2}$ | -0.3 to +23 | V |
| LX/CS to PGND | $V_{H3}$ | -0.3 to +23 | V |
| LX/CS to GDI | $V_{H4}$ | -0.3 to +23 | V |
| GDI to AVDD | $V_{H5}$ | -0.3 to +23 | V |
| VL, OUTBK1, GATE to PGND | $V_{H6}$ | -0.3 to +6.0 | V |
| LXBK1 to PGND | $V_{H7}$ | -0.3 to (VIN_BK1+0.3) | V |
| DRVP/LXVGH, VGH to PGND | $V_{H8}$ | -0.3 to +50 | V |
| DRVN/LXVGL, VGL to PGND | $V_{L1}$ | -20 to +0.3 | V |
| DRVN/LXVGL to VIN_VGL | $V_{L2}$ | -40 to +0.3 | V |
| VSS1 to PGND | $V_{L3}$ | -20 to +0.3 | V |
| VSS1 to VGL | $V_{L4}$ | -0.3 to +15 | V |
| VGH to VGL, VSS1 | $V_{H9}$ | -0.3 to +60 | V |
| VGL to VSS1 | $V_{L5}$ | -20 to +0.3 | V |
| VCOM1, GMA1~14 to PGND | $V_{H10}$ | -0.3 to (VIN_GMA+0.3) | V |
| Thermal Resistance-junction to ambient (WQFN 6.5x4.5-46) | $\theta_{JA}$ | 28.6 | ℃/W |
| Thermal Resistance -junction to case (WQFN 6.5x4.5-46) | $\theta_{JC}$ | 11.6 | ℃/W |
| Power Dissipation, @ $T_A$ = +25℃, $T_J$= 125℃ | $P_D$ | 3.5 | W |
| Operating Ambient Temperature Range | $T_A$ | –40 to +85 | ℃ |
| Operating Junction Temperature Range | $T_J$ | –40 to +150 | ℃ |
| Storage Temperature Range | $T_{STORAGE}$ | –65 to +150 | ℃ |
| ESD Susceptibility Human Body Mode | HBM | 2500 | V |
| ESD Susceptibility Machine Mode | MM | 200 | V |

Note:
1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.
2. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# ELECTRICAL CHARACTERISTICS

(VIN =5/12V, $V_{BK1}$=3.3V, $V_{AVDD}$=16V, $V_{HAVDD}$=8V, VGH=28V, VGL= -10V, VSS1=-6V, $T_A$ = 0℃ to 85℃, unless otherwise specified. Typical values are tested at +25℃ ambient temperature)

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **General** | | | | | | |
| $V_{IN}$ | Input voltage range | VIN=12V, REG46h [7] =0 | 8.6 | -- | 14.7 | V |
| | | VIN=5V, REG46h [7] =1 | 4.4 | -- | 6.0 | V |
| $I_Q$ | Quiescent current into VIN_BK1 | No switching | -- | 3.5 | -- | mA |
| | Quiescent current into VIN_VGL | No switching | -- | 3 | -- | mA |
| | Quiescent current into VIN_GMA | No switching | -- | 8 | -- | mA |
| $V_{UVLO\_12V}$ | Under voltage lockout threshold | VIN rising | -- | 8.3 | -- | V |
| | | VIN falling | -- | 7.5 | -- | V |
| $V_{UVLO\_5V}$ | Under voltage lockout threshold | VIN rising | -- | 4.3 | -- | V |
| | | VIN falling | -- | 4.0 | -- | V |
| $V_L$ | $V_L$ output voltage | VIN= 8.6V ~ 14.7V | 4.9 | 5.0 | 5.1 | V |
| **VT Function** | | | | | | |
| $V_{VT\_HT}$ | VT_HT adjustable threshold | 4 bits, step=0.2V | 0.4 | -- | 3.4 | V |
| $V_{VT\_LT}$ | VT_LT adjustable threshold | 4 bits, step=0.2V | 0.4 | -- | 3.4 | V |
| **Protections** | | | | | | |
| $T_{SD}$ | Thermal shutdown | rising | -- | 150 | -- | ℃ |
| $V_{OVP\_AVDD}$ | AVDD over voltage protection threshold | $V_{GDI}$ rising | -- | 21.25 | -- | V |
| $HY_{OVP\_AVDD}$ | AVDD over voltage protection hysteresis | $V_{OVP\_L}$(OVP threshold low) =$V_{OVP\_H}$-$HY_{OVP}$ | -- | 0.5 | -- | V |
| $V_{OVP1}$ | Over voltage protection threshold | For BK1, HAVDD | -- | 120 | -- | % |
| $HY_{OVP1}$ | Over voltage protection hysteresis | $V_{OVP\_L}$(OVP threshold low) =$V_{OVP\_H}$-$HY_{OVP}$ For BK1 | -- | 15 | -- | % |
| $t_{OVP\_HAVDD}$ | Duration to OVP trigger time | For HAVDD, latched off after delay time. | -- | 50 | -- | ms |
| $V_{UVP}$ | Under voltage protection threshold | For AVDD, VGH, VBK1, HAVDD, VGL, VSS1 | -- | 80 | -- | % |
| $t_{UVP}$ | Duration to UVP trigger time | For AVDD, VGH, VBK1, HAVDD, VGL, VSS1 | -- | 50 | -- | ms |
| $V_{SCP1}$ | Short circuit protection level 1 | For VGL, HAVDD | -- | 20 | -- | % |
| $V_{SCP2}$ | Short circuit protection level 2 | For AVDD, VBK1, VGH | -- | 40 | -- | % |
| **AVDD Step-up Regulator** | | | | | | |
| $V_{AVDD}$ | AVDD output voltage range | REG46h [7] =0 | 13.5 | -- | 19.8 | V |
| | | REG46h [7] =1 | 11 | -- | 17.3 | V |
| $V_{AVDD\_ACC}$ | AVDD output voltage accuracy | No load, Default output (16V) | -1.0 | -- | 1.0 | % |
| $f_{LX\_AVDD}$ | AVDD switching frequency | REG29h [7] =0 | -- | 750 | -- | kHz |
| | | REG29h [7] =1 | -- | 500 | -- | kHz |

| | | | | | | |
|---|---|---|---|---|---|---|
| $R_{ON\_LX}$ | AVDD built-in NMOS switch on-resistance | $I_{LX/CS}$=500mA | -- | 100 | -- | mΩ |
| $R_{ON\_DMP}$ | AVDD Damping switch on-resistance | | | 4 | | Ω |
| GM | Transconductance | | -- | 200 | -- | μA/V |
| $R_{CS}$ | Current-sense trans resistance | | -- | 0.25 | -- | Ω |
| $I_{LEAK\_LX/CS}$ | LX/CS NMOS leakage current | $V_{LX/CS}$=19.8V | -- | 1 | 10 | μA |
| $I_{LIM\_LX/CS}$ | LX/CS NMOS switch current limit | AVDD OCP | 5 | -- | -- | A |
| $D_{MAX\_LX/CS}$ | LX/CS Maximum Duty Cycle | | 82 | 88 | 94 | % |
| | Line regulation | 8.6V≤VIN≤14.7V, $I_{AVDD}$=1mA | -- | 0.04 | -- | %/V |
| | Load regulation | 1mA ≤ $I_{AVDD}$ ≤ 1.5A | -1.0 | -- | +1.0 | % |
| $t_{SS\_AVDD}$ | AVDD soft-start time | REG2Dh [1] =0 | -- | 10 | -- | ms |
| | | REG2Dh [1] =1 | -- | 20 | -- | ms |
| $R_{DIS\_AVDD}$ | AVDD discharge resistance | | -- | 4.7 | -- | kΩ |
| **AVDD External Driver** | | | | | | |
| $V_{GATE\_ON}$ | AVDD N-MOSFET gate driver | On level | 4.5 | 5.0 | 5.5 | V |
| $V_{GATE\_OFF}$ | | Off level | 0 | -- | 0.3 | V |
| $V_{CS\_OCP}$ | External NMOS switch current limit | $R_{CS}$=50mΩ | -- | 0.3 | -- | V |
| $R_{DSON\_GH}$ | Gate to VL high-side on resistance | | -- | 5 | -- | Ω |
| $R_{DSON\_GL}$ | Gate to GND low-side on resistance | | -- | 5 | -- | Ω |
| $V_{GD\_H}$ | GD (isolated switch) driver | Pull high | -- | GDI | -- | V |
| $V_{GD\_L}$ | | Pull low | -- | GDI-6 | -- | V |
| $R_{GD}$ | GD pull high resistor | | -- | 6.4 | -- | kΩ |
| $I_{GD\_SINK}$ | GD sink current | | -- | 10 | -- | μA |
| **VGH Step-up Regulator** | | | | | | |
| $V_{GH\_NT}$ | VGH output voltage range | 5 bits, step=1V | 20 | -- | 45 | V |
| $V_{GH\_LT}$ | VGH_LT output voltage range | 5 bits, step=1V | 20 | -- | 45 | V |
| $V_{GH\_ACC}$ | VGH voltage accuracy | VGH=28V, no load | -3.0 | -- | +3.0 | % |
| $f_{LX\_VGH}$ | VGH switching frequency | REG29h [7] =0 | -- | 750 | -- | kHz |
| | | REG29h [7] =1 | -- | 500 | -- | kHz |
| $MIN_{\_LXVGH}$ | LXVGH minimum on time | | -- | 100 | -- | ns |
| $R_{ON\_LXVGH}$ | LXVGH low side switch on-resistance | | -- | 0.5 | -- | Ω |
| $I_{LEAK\_LXVGH}$ | LXVGH NMOS leakage current | $V_{LXVGH}$=45V | -- | 1 | -- | μA |
| $I_{LIM\_LXVGH}$ | LXVGH NMOS switch current limit | | 1.5 | -- | -- | A |
| $D_{MAX\_LXVGH}$ | LXVGH Maximum Duty Cycle | | 82 | 88 | 94 | % |
| | Line regulation | 8.6V≤VIN≤14.7V, $I_{VGH}$=1mA | -- | 0.2 | -- | % |
| | Load regulation | 1mA ≤ $I_{VGH}$ ≤ 0.3A | -1.0 | -- | +1.0 | % |
| $t_{SS\_VGH}$ | VGH soft-start time | REG2Dh [0] =0 | -- | 3 | -- | ms |
| | | REG2Dh [0] =1 | -- | 6 | -- | ms |
| $R_{DIS\_VGH}$ | VGH discharge resistance | | -- | 30 | -- | kΩ |
| **VGH Positive Charge-pump Regulator** | | | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{GH\_NT}$ | VGH output voltage range | 5 bits, step=1V | 20 | -- | 45 | V |
| $V_{GH\_LT}$ | VGH_LT output voltage range | 5 bits, step=1V | 20 | -- | 45 | V |
| $V_{GH\_ACC}$ | VGH voltage accuracy | VGH=28V, no load | -3.0 | -- | +3.0 | % |
| $I_{LEAK\_DRVP}$ | DRVP leakage current | $V_{DRVP}$=45V | -- | 1 | 10 | μA |
| $I_{DRVP}$ | DRVP sink current | | -- | 5 | -- | mA |
| | Line regulation | 8.6V≤VIN≤14.7V, $I_{VGH}$=0.1A | -- | 0.1 | -- | % |
| | Load regulation | 1mA ≤ $I_{VGH}$ ≤ 0.15A | -3.0 | -- | +3.0 | % |
| $t_{SS\_VGH}$ | VGH soft-start time | REG2Dh [0] =0 | -- | 3 | -- | ms |
| | | REG2Dh [0] =1 | -- | 6 | -- | ms |
| $R_{DIS\_VGH}$ | VGH discharge resistance | | -- | 30 | -- | kΩ |
| **VBK1 Step-down Regulator** | | | | | | |
| VBK1 | VBK1 output voltage range | 5 bits, step=50mV | 1.8 | -- | 3.35 | V |
| $V_{BK1\_ACC}$ | VBK1 voltage accuracy | VBK1=3.3V, no load | -2.0 | -- | +2.0 | % |
| $f_{LX\_BK1}$ | VBK1 switching frequency | REG29h [7] =0 | -- | 750 | -- | kHz |
| | | REG29h [7] =1 | -- | 500 | -- | kHz |
| $MIN_{\_LXVGH}$ | LX_BK1 minimum on time | | -- | 100 | -- | ns |
| $R_{ON\_BK1\_HS}$ | LX_BK1 high side PMOS switch on-resistance | $I_{LX\_BK1}$=500mA | -- | 400 | -- | mΩ |
| $R_{ON\_BK1\_LS}$ | LX_BK1 low side NMOS switch on-resistance | $I_{LX\_BK1}$= -500mA | -- | 200 | -- | mΩ |
| $I_{LEAK\_BK1\_HS}$ | LX_BK1 PMOS leakage current | $V_{LX\_BK1}$=0V | -- | 1 | 10 | μA |
| $I_{LEAK\_BK1\_LS}$ | LX_BK1 NMOS leakage current | $V_{LX\_BK1}$=12V | -- | 1 | -- | μA |
| $I_{LIM\_BK1}$ | LX_BK1 PMOS switch current limit | | 1.5 | -- | -- | A |
| $D_{MAX\_LX\_BK1}$ | LX_BK1 Maximum Duty Cycle | | 82 | 88 | 94 | % |
| | Line regulation | 8.6V≤VIN≤14.7V, $I_{BK1}$=500mA | -- | 0.2 | -- | % |
| | Load regulation | 1mA ≤ $I_{BK1}$ ≤ 1.5A | -1.0 | -- | 1.0 | % |
| $t_{SS\_BK1}$ | VBK1 soft-start time | | -- | 3 | -- | ms |
| $R_{DIS\_BK1}$ | VBK1 discharge resistance | | -- | 1 | -- | kΩ |
| **HAVDD OP Amplifier** | | | | | | |
| $V_{HAVDD}$ | HAVDD output voltage resolution | | -- | 7 | -- | bits |
| INL | Integral nonlinearity | No load | -4 | -- | +4 | LSB |
| DNL | Differential nonlinearity | No load | -1 | -- | +1 | LSB |
| $V_{OH}$ | HAVDD output voltage swing high | $I_{HAVDD}$= +100mA | -- | $V_{AVDD}$-2 | -- | V |
| $V_{OL}$ | HAVDD output voltage swing low | $I_{HAVDD}$= -100mA | -- | 2 | -- | V |
| $I_{SC}$ | HAVDD short circuit current | HAVDD to AVDD or PGND | -- | +/-200 | -- | mA |
| CMRR | Input common-mode rejection ratio | AVDD=15V, F=10kHz, 2V amplitude sin signal | -- | 80 | -- | dB |
| PSRR | Power supply rejection ratio | AVDD sweeps from 8V to 18V | -- | 60 | -- | dB |
| SR | Slew rate | | -- | 45 | -- | V/μs |
| BW | -3dB bandwidth | | -- | 20 | -- | MHz |
| | Load regulation | -100mA ≤ $I_{HAVDD}$ ≤ +100mA | -0.5 | -- | +0.5 | % |
| $R_{DIS\_HAVDD}$ | HAVDD discharge resistance | | -- | 10 | -- | kΩ |
| **VGL Inverting Regulator** | | | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{GL\_NT}$ | VGL output voltage range | 5 bits, step=0.5V | -18 | -- | -3 | V |
| $V_{GL\_LT/HT}$ | VGL_LT/HT output voltage range | 5 bits, step=0.5V | -18 | -- | -3 | V |
| $V_{GL\_ACC}$ | VGL voltage accuracy | VGL=-10V, no load | -3.0 | -- | +3.0 | % |
| $f_{LX\_VGL}$ | VGL switching frequency | REG29h [7] =0 | -- | 750 | -- | kHz |
| | | REG29h [7] =1 | -- | 500 | -- | kHz |
| $MIN_{\_LXVGL}$ | LXVGL minimum on time | | -- | 100 | -- | ns |
| $R_{ON\_LXVGL}$ | LXVGL PMOS switch on-resistance | $I_{LXVGL}$=100mA | -- | 0.65 | -- | Ω |
| $I_{LEAK\_LXVGH}$ | LXVGL PMOS leakage current | $V_{LXVGL}$=VIN or VGL | -- | 5 | -- | μA |
| $I_{LIM\_LXVGH}$ | LXVGL PMOS switch current limit | | 1.5 | -- | -- | A |
| $D_{MAX\_LXVGL}$ | LXVGL Maximum Duty Cycle | | 82 | 88 | 94 | % |
| | Line regulation | 8.6V≤VIN≤14.7V, $I_{VGL}$=0.1A | -- | 0.2 | -- | % |
| | Load regulation | 1mA ≤ $I_{VGL}$ ≤ 200mA | -1.0 | -- | +1.0 | % |
| $t_{SS\_VGL}$ | VGL soft-start time | | -- | 3 | -- | ms |
| $R_{DIS\_VGL}$ | VGL discharge resistance | | -- | 10 | -- | kΩ |
| **VGL Negative Charge-pump Regulator** | | | | | | |
| $V_{GL\_NT}$ | VGL output voltage range | 5 bits, step=0.5V | -18 | -- | -3 | V |
| $V_{GL\_LT/HT}$ | VGL_LT/HT output voltage range | 5 bits, step=0.5V | -18 | -- | -3 | V |
| $V_{GL\_ACC}$ | VGL voltage accuracy | VGL=-10V, no load | -3.0 | -- | +3.0 | % |
| $I_{LEAK\_DRVN}$ | DRVN leakage current | $V_{DRVN}$=-15V | -1 | 1 | 10 | μA |
| $I_{DRVN}$ | DRVN source current | | -- | 10 | -- | mA |
| | Line regulation | 8.6V≤VIN≤14.7V, $I_{VGL}$=0.1A | -- | 0.1 | -- | % |
| | Load regulation | 1mA ≤ $I_{VGL}$ ≤ 150mA | -3.0 | -- | +3.0 | % |
| $t_{SS\_VGL}$ | VGL soft-start time | | -- | 3 | -- | ms |
| $R_{DIS\_VGL}$ | VGL discharge resistance | | -- | 10 | -- | kΩ |
| **VSS1 Negative Linear Regulator** | | | | | | |
| VSS1 | VSS1 output voltage range | 5 bits, step=0.5V | -16 | -- | -3 | V |
| $V_{SS1\_ACC}$ | VSS1 output voltage accuracy | VSS1=-6V, No load | -3.0 | -- | +3.0 | % |
| $I_{LIM\_VSS1}$ | VSS1 current limit threshold | Sourcing and sink load | -- | 100 | -- | mA |
| | Load regulation | -50mA ≤ $I_{VSS1}$ ≤ +50mA | -- | +/-1.5 | -- | mV/mA |
| $t_{SS\_VSS1}$ | VSS1 soft-start time | | -- | 3 | -- | ms |
| $R_{DIS\_VSS1}$ | VSS1 discharge resistance | | -- | 1.2 | -- | kΩ |
| **Programmable VCOM1 Buffers & VCOM2 DAC (VCOM1 & VCOM2)** | | | | | | |
| VIN_GMA | Supply range | | 13.5 | -- | 19.8 | V |
| $V_{COM1}$/ $V_{COM2DAC}$ | VCOM output voltage range | VCOM1 & VCOM2DAC will be clamped between VCOM_MAX and VCOM_MIN | PGND +0.5V | -- | $V_{AVDD}$ -0.5V | V |
| $V_{COM1}$/ $V_{COM2DAC}$ | VCOM output voltage | VCOM DAC= 0 ~ 127 | VCOM_MIN+VCOM[7:1]* ((VCOM_MAX-VCOM_MIN)/127) | | | V |
| $V_{VCOM\_MAX}$ | VCOM Max output voltage | 7 bits | ($V_{AVDD}$/128)* (VCOM_MAX[6:0]+1) | | | V |
| $V_{VCOM\_MIN}$ | VCOM Max output voltage | 7 bits | $V_{AVDD}$/128* (VCOM_MIN[6:0]) | | | V |
| | VCOM1 & VCOM2DAC voltage resolution | VCOM1 & VCOM2DAC will be clamped between | -- | 7 | -- | bits |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | VCOM_MAX and VCOM_MIN | | | | |
| INL | Integral nonlinearity | No load | -4 | -- | +4 | LSB |
| DNL | Differential nonlinearity | No load | -1 | -- | +1 | LSB |
| $I_{SC\_VCOM1}$ | VCOM1 short circuit current | VCOM1 short to VIN_GMA or PGND | -- | +/-400 | -- | mA |
| $t_{DLY\_VCOM1}$ $t_{DLY\_VCOM2DAC}$ | Program to output delay | From ACK falling edge to programming VCOM change 50% voltage at output | -- | 1 | -- | µs |
| SR | VCOM1 slew rate | VCOM1: 10% <-> 90% | -- | 30 | -- | V/µs |
| | Load regulation | -100mA ≤$I_{VCOM1}$ ≤ +100mA | -1 | +/-0.5 | +1 | mV/mA |
| $R_{DIS\_VCOM1}$ | VCOM1 discharge resistance | 2 bits, Disable/20Ω/1kΩ/8kΩ | Disable | -- | 8 | kΩ |
| **14-Channel Programmable Gamma Buffers (GMA1 ~ GMA 14)** | | | | | | |
| VIN_GMA | Supply range | | 13.5 | -- | 19.8 | V |
| | Gamma voltage resolution | GMA1~14 | -- | 10 | -- | bits |
| $V_{GMA\_RNG}$ | Gamma output voltage range | $I_{GMAx}$ = sink or sourcing 5mA | PGND +0.2V | -- | $V_{AVDD}$ -0.2V | V |
| $V_{GMAx}$ | Gamma output voltage | | $V_{AVDD}$*((GMAx[9:0])/1024) | | | V |
| INL | Integral nonlinearity | No load | -4 | -- | +4 | LSB |
| DNL | Differential nonlinearity | No load | -1 | -- | +1 | LSB |
| $I_{GMA}$ | Gamma output current | VGMAx drop 0.5V | -- | +/-50 | -- | mA |
| $I_{SC\_GMA}$ | Gamma short circuit current | VGMAx short to VIN_GMA or PGND | -- | +/-100 | -- | mA |
| $t_{DLY\_GMA}$ | Program to output delay | From ACK falling edge to programming Gamma change 50% voltage at output | -- | 15 | -- | µs |
| SR | Gamma slew rate | GMAx: 10% <-> 90% | -- | 15 | -- | V/µs |
| | Load regulation | -12mA ≤$I_{GMAx}$ ≤ +12mA | -- | +/-0.5 +Rd | -- | mV/mA |
| **LOGIC SIGNALS EN, SCL, SDA and FAULT** | | | | | | |
| $V_{IH}$ | EN/SCL/SDA logic high level voltage | | 1.6 | -- | -- | V |
| $V_{IL}$ | EN/SCL/SDA logic low level voltage | | -- | -- | 0.6 | V |
| $V_{IH\_FAULT}$ | FAULT logic high level voltage | | 2.0 | -- | -- | V |
| $V_{IL\_FAULT}$ | FAULT logic low level voltage | | -- | -- | 1.0 | V |
| $I_{IH}$, $I_{IL}$ | SCL/SDA input leakage current | $V_I$=0V or 3.3V | -1 | 0.01 | 1 | µA |
| $R_{PD\_EN}$ | EN pull-down resistance | | 320 | 400 | 480 | kΩ |
| $R_{PU\_FAULT}$ | FAULT pull-high resistance | | -- | 100 | -- | kΩ |
| | FAULT On voltage | $I_{IN}$=3mA | -- | -- | 0.5 | V |
| **I2C Interface** | | | | | | |
| $C_{SI}$ | SLC, SDA input capacitance | | -- | 5 | -- | pF |
| $V_{OL\_SDA}$ | SDA output low voltage | $I_{SINK}$=6mA | -- | -- | 0.3 | V |
| $f_{SCL}$ | SCL clock frequency | | 1 | -- | 400 | kHz |
| $t_{LOW}$ | LOW period of the SCL clock | | 1.3 | -- | -- | µs |

| | | | | | | |
|---|---|---|---|---|---|---|
| $t_{HIGH}$ | HIGH period of the SCL clock | | 600 | -- | -- | ns |
| $t_{BUF}$ | Bus free time between a STOP and a START condition | | 1300 | -- | -- | ns |
| $t_{HD;STA}$ | Hold time for a repeated START condition | | 600 | -- | -- | ns |
| $t_{SU;STA}$ | Setup time for a repeated START condition | | 600 | -- | -- | ns |
| $t_{SU;DAT}$ | Data setup time | | 100 | -- | -- | ns |
| $t_{HD;DAT}$ | Data hold time | | 50 | -- | 900 | ns |
| $t_{SU;STO}$ | Setup time for STOP condition | | 600 | -- | | ns |
| $t_R$ | Input rise time (SCL & SDA) | (Note 1) | 20+ $0.1C_B$ | -- | 300 | µs |
| $t_F$ | Input fall time (SCL & SDA) | (Note 1) | 20+ $0.1C_B$ | -- | 300 | ns |
| $t_F$ | SDA Transmitting fall time | (Note 1) | 20+ $0.1C_B$ | -- | 250 | ns |
| $t_{SP}$ | Pulse width of suppressed spike | | 0 | -- | 50 | ns |
| $C_B$ | Capacitive load for SDA and SCL | | -- | -- | 0.4 | nF |
| | EEPROM start up blanking time | IC power up initialize (Note 2) | -- | 30 | 40 | ms |
| | Program EEPROM blanking time | (Note 2) | -- | 30 | 40 | ms |
| | Read EEPROM blanking time | (Note 2) | -- | 1.5 | 5 | ms |

**Note 1**: $C_B$ is in pF.
**Note 2**: The blanking time is defined as the duration of $I^2C$ REG write to or load from EEPROM.
**Note 3**: For boost converter application. Output voltage must larger than input voltage, so (AVDD- VIN) must larger than 1.5V.(AVDD–VIN > 1.5V)

# THEORY OF OPERATION

The iML1942 is an I2C programmable solution for TV&MNT LCD panels. The device consists of one current mode boost regulator for AVDD, one synchronous buck converter for VBK1. An optional boost regulator or charge-pump regulator for VGH with temperature-compensated, one optional inverting converter or negative charge-pump regulator for VGL with temperature-compensated, a negative linear regulator (VSS1), a programmable high-current operational amplifiers for VCOM1, a programmable DAC for VCOM2DAC and 14-channel programmable gamma buffers.

## AVDD Main Step-Up Regulator-Optional Internal/External NMOS Drive.

The main step-up regulator provides the regulated supply voltage (Internal/External Control) for the panel source driver ICs. It employs a current-mode, programmable frequency PWM architecture to maximize loop bandwidth and provide fast-transient response. The regulator operates at a programmable switching frequency (500kHz/750kHz selectable) to minimize external components and enhance efficiency. One bit of Fsw is used to adjust switching frequency including step-up regulator, step-down regulator. The AVDD output voltage is adjustable through $I^2C$. Refer to the "*$I^2C$ Interface Register Map*" section for details.

### Loop Compensation

A series RC on the COMP pin is needed to stabilize the loop. Choose $R_{COMP}$ to set the high-frequency integrator gain for fast transient response and choose $C_{COMP}$ to set the integrator zero to maintain loop stability (figure 1). Start the compensation values as suggested by the application circuit and adjust as needed. To further optimize transient response, vary $R_{COMP}$ in 20% steps and $C_{COMP}$ in 50% steps while observing transient response waveforms.

## Adjustable Soft-start Time

The iML1942 provides one bit by $I^2C$ to adjust AVDD soft-start time of main step-up regulator. Refer to the "Register Map" section for details.

## VB1 Synchronous Step-Down Regulator

The iML1942 integrates one step-down regulators that is typically used for I/O and core voltage. The output voltage can be set through $I^2C$ and details can be referred to definition of respective registers. VBK1 have one bit (500kHz/750kHz selectable) is used to adjust switching frequency. The high switching frequency can minimize inductor size and use less output capacitance to acquire the same performance. The regulators feature a 3ms fixed soft start time to minimize inrush current at startup.

## VGH Optional Boost Regulator or Positive Charge-pump Regulator

The iML1942 includes an optional boost regulator or positive charge-pump with temperature-compensated output. VGH have one bit is used to adjust the structure type of VGH. Its output can also be set through $I^2C$ and details can be

referred to definition of respective registers.

The VGH regulator includes temperature compensation function. The voltage ($V_T$) at the NTC Pin will adjust the reference voltage. At the non-inverting input of the error amplifier. This reference voltage will also adjust the VGH regulation voltage, and therefore tune the output voltage. The output voltage is compensated accordingly. The Voltage step resolution is 4 bits from high boundary Voltage to low boundary VGH voltage. (see Fig 3.) VGH TC function is enable by programming register VGH_LT_EN (0x04h bit[7])=1. For conditions where the temperature is $T_B \leqq T_A \leqq T_C$, as shown in the temperature compensation Table1 below.

| °C / V | $T_A < T_2$ | $T_2 \leqq T_A \leqq T_1$ | $T_A > T_1$ |
|---|---|---|---|
| $V_{NTC}$ | VTC2 | $V_T$ | VTC1 |
| VGH | VGH Voltage_ LT Register | Dependent on external $R_{NTC}$ network | VGH Register |

Table1. Temperature-compensated VGH with varying $V_T$

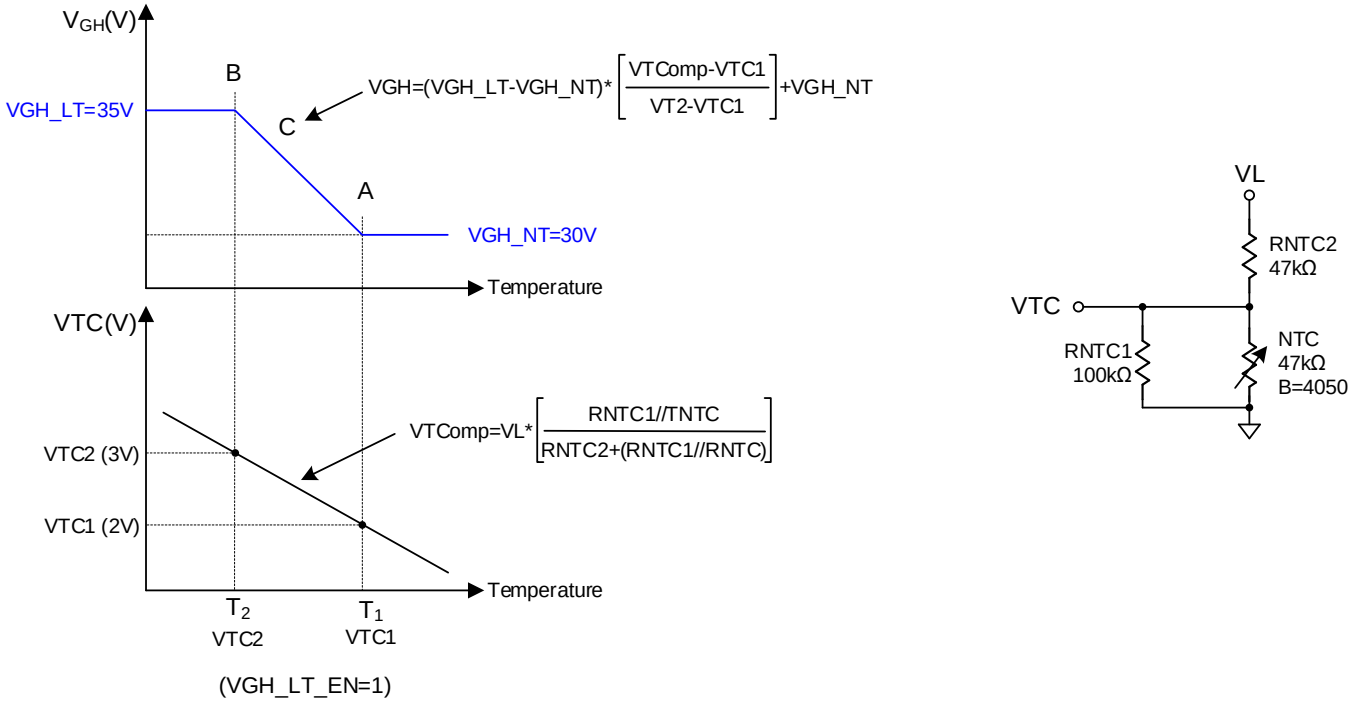



Figure 4. VGH Temperature Compensation Characteristic

## VGL Optional Inverting Regulator or Negative Charge-pump Regulator

The VGL regulator in iML1942 is an optional inverting regulator or negative charge-pump. It also includes temperature-compensated output which is set by I²C. The voltage ($V_T$) at the NTC Pin will adjust the reference voltage. At the non-inverting input of the error amplifier. This reference voltage will also adjust the VGL regulation voltage, and therefore tune the output voltage. The output voltage is compensated accordingly. The Voltage step resolution is 4 bits from high boundary Voltage to low boundary VGL voltage. (See Fig 4.) VGL TC function is enable by programming both register VGL_LT/HT_EN (0x06h bit[7])=1 and register VGL_LT/HT_SEL(0x06h bit[6]). For conditions where the temperature is $T_B \leqq T_A \leqq T_C$, as shown in the temperature compensation Table1 below.

| °C / V | | $T_A < T_2$ | $T_2 \leqq T_A \leqq T_1$ | $T_A > T_1$ |
|---|---|---|---|---|
| $V_{NTC}$ | | VTC2 | VTC2≦ $V_T$ ≦VTC1 | VTC1 |
| VGL | VGL_LT/HT_SEL=0 | VGL Voltage LT Register | Dependent on external $R_{NTC}$ network | VGL Register |
| | VGL_LT/HT_SEL=1 | VGL Register | Dependent on external $R_{NTC}$ network | VGL Voltage HT Register |

Table2. Temperature-compensated VGL with varying $V_T$

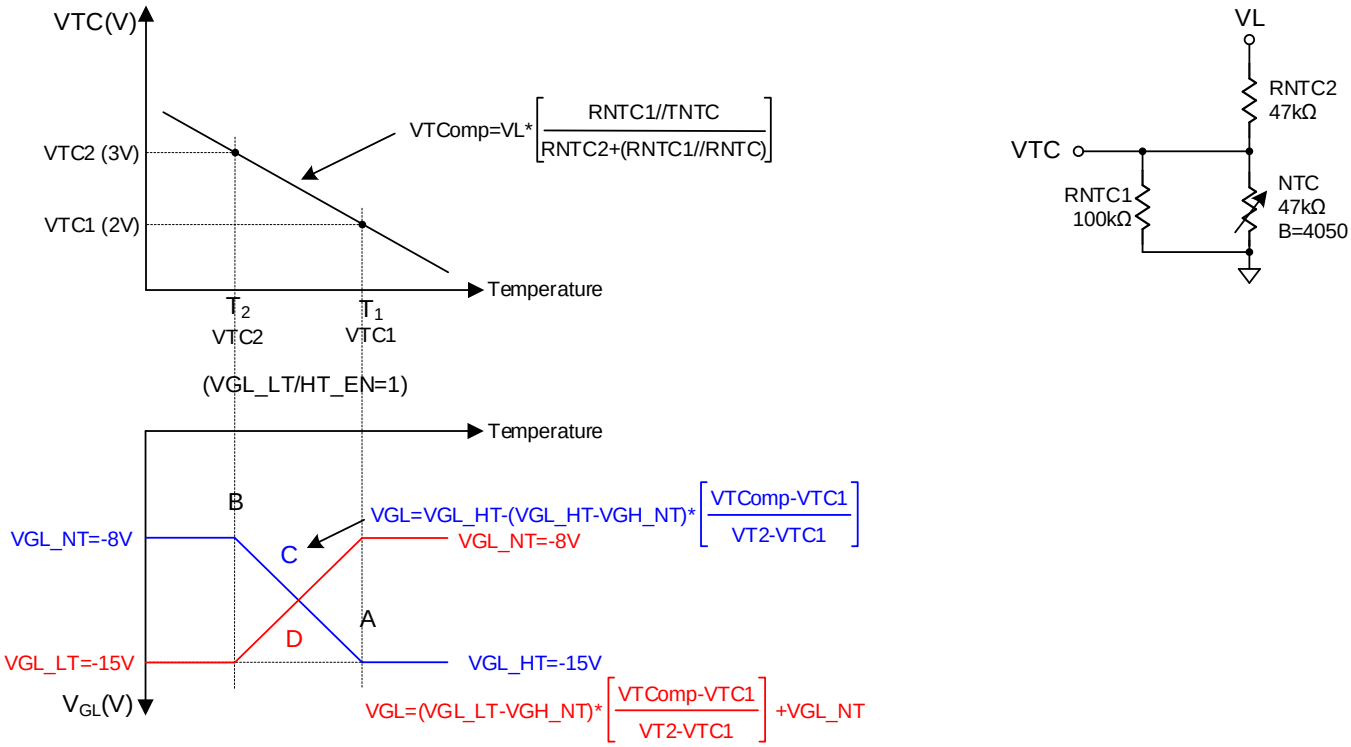



Figure 4. VGL Temperature Compensation Characteristic

## VSS1 Linear Regulator

The iML1942 provides a negative voltage linear regulator for VSS1 for level-shifters. Like other regulators, its output is programmable by I²C. Refer to register map for more details. The VSS1 regulator can provide sourcing and sinking capacity which can be up to at least +/- 100mA current capacity.

## VCOM1 Operational Amplifiers

The iML1942 includes one channel VCOM1 amplifiers and be used to drive the LCD backplane. The amplifier includes 7-bit DAC to program voltage level between 0V and $V_{AVDD}$ (set by registers) accordingly. The amplifier is capable of sourcing and sinking capacitive pulse currents which can occur when the TFT source voltage changes. It features up to at least ±400mA (min.) output short-circuits current.

## 14-channel Programmable Gamma Reference Buffers

The iML1942 includes I²C interfaced digitally programmable gamma buffers featuring 10-bit DACs for excellent resolution. The programmable gamma reference buffers are designed to improve the characteristics of the source drivers. The output voltage is determined by a 10-bit code set through the I²C interface set. Refer to the *Register Map* section for details. It features up to at least ±100mA (min.) output short-circuits current.

# Fault Protection Table

The iML1942 includes different protections to prevent the device from damage.
Fault protection table and fault are shown in table 1 and 2.

| | OVP | | UVP | | SCP | |
|---|---|---|---|---|---|---|
| Channel | OVP Threshold | Delay time | UVP Threshold | Delay time | SCP Threshold | Delay time |
| VBK1 | Vtyp=120% | immediate | Vtyp=80% | 50ms | Vtyp=40% | immediate |
| AVDD | Vtyp=21.25V | immediate | Vtyp=80% | 50ms | Vtyp=40% | immediate |
| HAVDD | Vtyp=120% | 50ms | Vtyp=80% | 50ms | Vtyp=20% | immediate |
| VGH | -- | immediate | Vtyp=80% | 50ms | Vtyp=40% | immediate |
| VGL | -- | immediate | Vtyp=80% | 50ms | Vtyp=20% | immediate |
| VSS1 | -- | -- | Vtyp=80% | 50ms | -- | -- |

Table 1. The iML1942 Fault Protection Table

| Channel Fault Condition | VBK1 | AVDD | HAVDD | VGH | VGL | VSS1 | GAMMA | VCOM1 | Condition to release protection |
|---|---|---|---|---|---|---|---|---|---|
| VBK1 OVP | Standby | O | O | O | O | O | O | O | $V_O < V_{TH\_OVP}$ - Hys |
| VBK1 UVP/SCP | X | X | X | X | X | X | X | X | Cycling VIN |
| AVDD OVP | O | Standby | O | O | O | O | O | O | $V_O < V_{TH\_OVP}$ - Hys |
| AVDD UVP/SCP | O | X | X | X | X | X | X | X | Cycling VIN |
| HAVDD OVP | O | X | X | X | X | X | X | X | Cycling VIN |
| HAVDD UVP/SCP | O | X | X | X | X | X | X | X | Cycling VIN |
| VGH OVP | O | O | O | Standby | O | O | O | O | $V_O < V_{TH\_OVP}$ - Hys |
| VGH UVP/SCP | O | X | X | X | X | X | X | X | Cycling VIN |
| VGL OVP | O | O | O | O | Standby | O | O | O | $V_O < V_{TH\_OVP}$ - Hys |
| VGL UVP/SCP | O | X | X | X | X | X | X | X | Cycling VIN |
| VSS1 UVP | O | X | X | X | X | X | X | X | Cycling VIN |
| Thermal (150℃) | X | X | X | X | X | X | X | X | Cycling VIN |

Table 2. The iML1942 Fault Behavior

# Application Information

## I²C Interface

The iML1942 features an I²C-comptabile, 2-wire serial interface consisting of a serial-data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the IC and the master device at clock rates up to 400kHz. The master generates the SCL clock signal and initiates data transfer on the bus. The master device writes data to the IC by transmitting the proper slave address followed by the register address and then the data byte. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each byte transmitted to the IC is followed by an acknowledge pulse.

## Slave Address

The slave address is one byte of data which is used as the unique identifier of the iML1942. The first 7 bits of the slave address are hard-coded and the least significant bit (LSB) of the slave address byte is the read/write (R/W) bit, which is used to determine whether a command is a write command or a read command. Set the R/W bit to 1 to configure the IC to read mode and to 0 to configure the IC to write mode. The slave address is the first byte of information sent to the IC after the START condition. Table 3 shows the slave addresses for the iML1942.

| Bit 7 | Bit 6 | Bit5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | $R/\overline{W}$ |

Table 3. Configuration Parameters Slave Address

| Bit 7 | Bit 6 | Bit5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | $R/\overline{W}$ |

Table 4. VCOM1 Slave Address

# REGISGER MAP

## PMIC Section

| Register Name | Address in Hex | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| AVDD Output Set | 0 | | | AVDD[5:0] | | | | | |
| VBK1 Output Set | 1 | VBK1_SYNC | | | VBK1[4:0] | | | | |
| HAVDD Output Set | 2 | | HAVDD[6:0] | | | | | | |
| VGH_NT Output Set | 3 | | | | VGH[4:0] | | | | |
| VGH_LT Output Set | 4 | VGH_LT_EN | | | VGH_LT[4:0] | | | | |
| VGL_NT Output Set | 5 | | | | VGL[4:0] | | | | |
| VGL_LT/HT Output Set | 6 | VGL_LT/HT_EN | VGL_LT/HT_SEL | | VGL_LT/HT[4:0] | | | | |
| VSS1 Output Set | 7 | | | | VSS1[4:0] | | | | |
| VCOM1 Voltage Set | 8 | VCOM1[8:0] | | | | | | | |
| VCOM MAX. Set | A | | VCOM_MAX[8:0] | | | | | | |
| VCOM MIN. Set | B | | VCOM_MIN[8:0] | | | | | | |
| GMA1 Output Set 1 | C | | | | | | | GMA1[9:8] | |
| GMA1 Output Set 2 | D | GMA1[7:0] | | | | | | | |
| GMA2 Output Set 1 | E | | | | | | | GMA2[9:8] | |
| GMA2 Output Set 2 | F | GMA2[7:0] | | | | | | | |
| GMA3 Output Set 1 | 10 | | | | | | | GMA3[9:8] | |
| GMA3 Output Set 2 | 11 | GMA3[7:0] | | | | | | | |
| GMA4 Output Set 1 | 12 | | | | | | | GMA4[9:8] | |
| GMA4 Output Set 2 | 13 | GMA4[7:0] | | | | | | | |
| GMA5 Output Set 1 | 14 | | | | | | | GMA5[9:8] | |
| GMA5 Output Set 2 | 15 | GMA5[7:0] | | | | | | | |
| GMA6 Output Set 1 | 16 | | | | | | | GMA6[9:8] | |
| GMA6 Output Set 2 | 17 | GMA6[7:0] | | | | | | | |
| GMA7 Output Set 1 | 18 | | | | | | | GMA7[9:8] | |
| GMA7 Output Set 2 | 19 | GMA7[7:0] | | | | | | | |
| GMA8 Output Set 1 | 1A | | | | | | | GMA8[9:8] | |
| GMA8 Output Set 2 | 1B | GMA8[7:0] | | | | | | | |
| GMA9 Output Set 1 | 1C | | | | | | | GMA9[9:8] | |
| GMA9 Output Set 2 | 1D | GMA9[7:0] | | | | | | | |
| GMA10 Output Set 1 | 1E | | | | | | | GMA10[9:8] | |
| GMA10 Output Set 2 | 1F | GMA10[7:0] | | | | | | | |
| GMA11 Output Set 1 | 20 | | | | | | | GMA11[9:8] | |
| GMA11 Output Set 2 | 21 | GMA11[7:0] | | | | | | | |
| GMA12 Output Set 1 | 22 | | | | | | | GMA12[9:8] | |
| GMA12 Output Set 2 | 23 | GMA12[7:0] | | | | | | | |
| GMA13 Output Set 1 | 24 | | | | | | | GMA13[9:8] | |
| GMA13 Output Set 2 | 25 | GMA13[7:0] | | | | | | | |
| GMA14 Output Set 1 | 26 | | | | | | | GMA14[9:8] | |
| GMA14 Output Set 2 | 27 | GMA14[7:0] | | | | | | | |
| Channel On/Off Set 1 | 28 | Group B_EN | VGL_EN | VSS1_EN | AVDD_EN | HAVDD_EN | GMA_EN | VCOM1_EN | VGH_EN |
| Channel Set 1 | 29 | FREQ_SEL | | | AVDD_NMOS_INT/EXT | VGH_TYPE | VGL_TYPE | VGL_PUMP_SOURCE | GMA_CH_TYPE |
| Delay Time Set 1 | 2A | | | DLY1_VBK1[1:0] | | DLY2_VGL[1:0] | | DLY3_VSS1[1:0] | |
| Delay Time Set 2 | 2B | | DLY4_AVDD[1:0] | | DLY5_VGH[1:0] | | DLY6_VCOM[2:0] | | |
| Discharge Resistor Set | 2C | ALL_DIS_EN | BK1_DIS | AVDD_DIS | VGH_DIS | VGL_DIS | HAVDD_DIS | VCOM1_DIS | |
| PMIC Conf. 1 | 2D | VSS1_EN | | | VCOM1_DIS_TYP | HAVDD_FB | | AVDD_SS | VGH_SS |
| VGH&VGL_VTC1/2 | 2E | VGH&VGL_VTC2[3:0] | | | | VGH&VGL_VTC1[3:0] | | | |
| PMIC Conf. 2 | 30 | | | AVDD_EXT_DRV[1:0] | | VGH_Boost_COMP[1:0] | | VGL_Inverting_COMP[1:0] | |
| PMIC Conf. 3 | 31 | EN_PIN_SEL | VCOM1_DLY_OFF | HAVDD_DLY_OFF | GMA_DLY_OFF | XON_DIS_THR[3:0] | | | |
| VCOM2DAC Set | 45 | VCOM2DAC[6:0] | | | | | | | |
| PMIC Conf. 4 | 46 | MNT_MODE_EN | | | | | | | VCOM2DAC_EN |
| EEPROM Control | FF | WR_NVM | WR_VCOM1 | | | | | | EE/DR |

## VCOM1 Section

| Register Name | Address in Hex | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| VCOM1 Conf. 1 | 0 | | | | RESET | VCOM1_WR_EPM | | OUT_EN | |
| VCOM1 Voltage Set | 1 | VCOM1[8:0] | | | | | | | |
| FAULT Flag | 2 | OTP | LS_NG | VBK1 UVP or SCP | AVDD UVP or SCP | VGH UVP or SCP | VGL UVP or SCP | VSS1 UVP | HAVDD UVP or SCP |

# GENERAL REGISTER DESCRIPTION

## Slaver Address (0x40h)

### AVDD Output Set (0x00h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| | 7 | W/R | 0 | Reserve. |
| | 6 | W/R | 0 | Reserve. |
| AVDD | 5 | W/R | 1 | (TV Mode): AVDD output voltage adjustment. 0.1V/Step from 13.5V to 19.8V. Default is 17.6V(29h).<br><br>(MNT Mode): AVDD output voltage adjustment. 0.1V/Step from 11.0V to 17.3V. Default is 15.1V(29h).<br><br>Refer to table below. |
| | 4 | W/R | 0 | |
| | 3 | W/R | 1 | |
| | 2 | W/R | 0 | |
| | 1 | W/R | 0 | |
| | 0 | W/R | 1 | |

#### TV Mode (REG46h[7]=0)

| Code | 0 | 1 | 10 | 11 | 100 | 101 | 110 | 111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| AVDD(V) | 13.5 | 13.6 | 13.7 | 13.8 | 13.9 | 14.0 | 14.1 | 14.2 | 14.3 | 14.4 | 14.5 | 14.6 | 14.7 | 14.8 | 14.9 | 15.0 |

| Code | 10000 | 10001 | 10010 | 10011 | 10100 | 10101 | 10110 | 10111 | 11000 | 11001 | 11010 | 11011 | 11100 | 11101 | 11110 | 11111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| HEX | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
| AVDD(V) | 15.1 | 15.2 | 15.3 | 15.4 | 15.5 | 15.6 | 15.7 | 15.8 | 15.9 | 16.0 | 16.1 | 16.2 | 16.3 | 16.4 | 16.5 | 16.6 |

| Code | 100000 | 100001 | 100010 | 100011 | 100100 | 100101 | 100110 | 100111 | 101000 | 101001 | 101010 | 101011 | 101100 | 101101 | 101110 | 101111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| HEX | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |
| AVDD(V) | 16.7 | 16.8 | 16.9 | 17.0 | 17.1 | 17.2 | 17.3 | 17.4 | 17.5 | 17.6 | 17.7 | 17.8 | 17.9 | 18.0 | 18.1 | 18.2 |

| Code | 110000 | 110001 | 110010 | 110011 | 110100 | 110101 | 110110 | 110111 | 111000 | 111001 | 111010 | 111011 | 111100 | 111101 | 111110 | 111111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 |
| HEX | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F |
| AVDD(V) | 18.3 | 18.4 | 18.5 | 18.6 | 18.7 | 18.8 | 18.9 | 19.0 | 19.1 | 19.2 | 19.3 | 19.4 | 19.5 | 19.6 | 19.7 | 19.8 |

#### MNT Mode (REG46h[7]=1)

| Code | 0 | 1 | 10 | 11 | 100 | 101 | 110 | 111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| AVDD(V) | 11.0 | 11.1 | 11.2 | 11.3 | 11.4 | 11.5 | 11.6 | 11.7 | 11.8 | 11.9 | 12.0 | 12.1 | 12.2 | 12.3 | 12.4 | 12.5 |

| Code | 10000 | 10001 | 10010 | 10011 | 10100 | 10101 | 10110 | 10111 | 11000 | 11001 | 11010 | 11011 | 11100 | 11101 | 11110 | 11111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| HEX | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
| AVDD(V) | 12.6 | 12.7 | 12.8 | 12.9 | 13.0 | 13.1 | 13.2 | 13.3 | 13.4 | 13.5 | 13.6 | 13.7 | 13.8 | 13.9 | 14.0 | 14.1 |

| Code | 100000 | 100001 | 100010 | 100011 | 100100 | 100101 | 100110 | 100111 | 101000 | 101001 | 101010 | 101011 | 101100 | 101101 | 101110 | 101111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| HEX | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |
| AVDD(V) | 14.2 | 14.3 | 14.4 | 14.5 | 14.6 | 14.7 | 14.8 | 14.9 | 15.0 | 15.1 | 15.2 | 15.3 | 15.4 | 15.5 | 15.6 | 15.7 |

| Code | 110000 | 110001 | 110010 | 110011 | 110100 | 110101 | 110110 | 110111 | 111000 | 111001 | 111010 | 111011 | 111100 | 111101 | 111110 | 111111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 |
| HEX | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B | 3C | 3D | 3E | 3F |
| AVDD(V) | 15.8 | 15.9 | 16.0 | 16.1 | 16.2 | 16.3 | 16.4 | 16.5 | 16.6 | 16.7 | 16.8 | 16.9 | 17.0 | 17.1 | 17.2 | 17.3 |

## VBK1 Output Set (0x01h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| VBK1_SYNC | 7 | W/R | 0 | 0: SYNC mode.<br>1: Asynchronous mode. |
| | 6 | W/R | 0 | Reserve. |
| | 5 | W/R | 0 | Reserve. |
| VBK1 | 4 | W/R | 1 | VBK1 output voltage adjustment. 0.05V/Step from 1.8V to 3.35V. Default is 3.30V(1Eh). Refer to table below. |
| | 3 | W/R | 1 | |
| | 2 | W/R | 1 | |
| | 1 | W/R | 1 | |
| | 0 | W/R | 0 | |

| Code | 0 | 1 | 10 | 11 | 100 | 101 | 110 | 111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| VBK1(V) | 1.80 | 1.85 | 1.90 | 1.95 | 2.00 | 2.05 | 2.10 | 2.15 | 2.20 | 2.25 | 2.30 | 2.35 | 2.40 | 2.45 | 2.50 | 2.55 |

| Code | 10000 | 10001 | 10010 | 10011 | 10100 | 10101 | 10110 | 10111 | 11000 | 11001 | 11010 | 11011 | 11100 | 11101 | 11110 | 11111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| HEX | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
| VBK1(V) | 2.60 | 2.65 | 2.70 | 2.75 | 2.80 | 2.85 | 2.90 | 2.95 | 3.00 | 3.05 | 3.10 | 3.15 | 3.20 | 3.25 | 3.30 | 3.35 |

## HAVDD Output Set (0x02h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| | 7 | W/R | 0 | Reserve. |
| HAVDD | 6 | W/R | 1 | (AVDD/512)*(HAVDD[6:0]+192)<br>HAVDD DAC = 0~127 |
| | 5 | W/R | 0 | |
| | 4 | W/R | 0 | |
| | 3 | W/R | 0 | |
| | 2 | W/R | 0 | |
| | 1 | W/R | 0 | |
| | 0 | W/R | 0 | |

## VGH_NT Output Set (0x03h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| | 7 | W/R | 0 | Reserve. |
| | 6 | W/R | 0 | Reserve. |
| | 5 | W/R | 0 | Reserve. |
| VGH | 4 | W/R | 0 | VGH output voltage adjustment. 1V/Step from 20V to 45V. Default is 30V(0Ah). Refer to table below. |
| | 3 | W/R | 1 | |
| | 2 | W/R | 0 | |
| | 1 | W/R | 1 | |
| | 0 | W/R | 0 | |

| Code | 0 | 1 | 10 | 11 | 100 | 101 | 110 | 111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| VGH(V) | 20.0 | 21.0 | 22.0 | 23.0 | 24.0 | 25.0 | 26.0 | 27.0 | 28.0 | 29.0 | 30.0 | 31.0 | 32.0 | 33.0 | 34.0 | 35.0 |

| Code | 10000 | 10001 | 10010 | 10011 | 10100 | 10101 | 10110 | 10111 | 11000 | 11001 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | | | | | | |
| HEX | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | | | | | | |
| VGH(V) | 36.0 | 37.0 | 38.0 | 39.0 | 40.0 | 41.0 | 42.0 | 43.0 | 44.0 | 45.0 | | | | | | |

## VGH_LT Output Set (0x04h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| VGH_LT_EN | 7 | W/R | 0 | VGH temperature compensation enable<br>0: Disable 1: Enable |
| | 6 | W/R | 0 | Reserve. |
| | 5 | W/R | 0 | Reserve. |
| VGH_LT | 4 | W/R | 0 | VGH_LT output voltage adjustment. 1V/Step from 20V to 45V. Default is 35V(0Fh). Refer to table below. |
| | 3 | W/R | 1 | |
| | 2 | W/R | 1 | |
| | 1 | W/R | 1 | |
| | 0 | W/R | 1 | |

| Code | 0 | 1 | 10 | 11 | 100 | 101 | 110 | 111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| VGH_LT(V) | 20.0 | 21.0 | 22.0 | 23.0 | 24.0 | 25.0 | 26.0 | 27.0 | 28.0 | 29.0 | 30.0 | 31.0 | 32.0 | 33.0 | 34.0 | 35.0 |

| Code | 10000 | 10001 | 10010 | 10011 | 10100 | 10101 | 10110 | 10111 | 11000 | 11001 |
|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 |
| HEX | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
| VGH_LT(V) | 36.0 | 37.0 | 38.0 | 39.0 | 40.0 | 41.0 | 42.0 | 43.0 | 44.0 | 45.0 |

## VGL_NT Output Set (0x05h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| | 7 | W/R | 0 | Reserve. |
| | 6 | W/R | 0 | Reserve. |
| | 5 | W/R | 0 | Reserve. |
| VGL | 4 | W/R | 0 | VGL output voltage adjustment. 0.5V/Step from -3V to -18V. Default is -8V(0Ah). Refer to table below. |
| | 3 | W/R | 1 | |
| | 2 | W/R | 0 | |
| | 1 | W/R | 1 | |
| | 0 | W/R | 0 | |

| Code | 0 | 1 | 10 | 11 | 100 | 101 | 110 | 111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| VGL(V) | -3.00 | -3.50 | -4.00 | -4.50 | -5.00 | -5.50 | -6.00 | -6.50 | -7.00 | -7.50 | -8.00 | -8.50 | -9.00 | -9.50 | -10.00 | -10.50 |

| Code | 10000 | 10001 | 10010 | 10011 | 10100 | 10101 | 10110 | 10111 | 11000 | 11001 | 11010 | 11011 | 11100 | 11101 | 11110 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | |
| HEX | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | |
| VGL(V) | -11.00 | -11.50 | -12.00 | -12.50 | -13.00 | -13.50 | -14.00 | -14.50 | -15.00 | -15.50 | -16.00 | -16.50 | -17.00 | -17.50 | -18.00 | |

## VGL_LT/HT Output Set (0x06h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| VGL_LT/HT_EN | 7 | W/R | 0 | VGL temperature compensation enable<br>0: Disable 1: Enable |
| VGL_LT/HT_SEL | 6 | W/R | 0 | VGL low or high temperature compensation selection<br>0: VGL_LT 1: VGL_HT |
| | 5 | W/R | 0 | Reserve. |
| VGL_LT/HT | 4 | W/R | 1 | VGL output voltage adjustment. 0.5V/Step from -3V to -18V. Default is -12V(12h). Refer to table below. |
| | 3 | W/R | 0 | |
| | 2 | W/R | 0 | |
| | 1 | W/R | 1 | |
| | 0 | W/R | 0 | |

| Code | 0 | 1 | 10 | 11 | 100 | 101 | 110 | 111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| VGL_LT/HT(V) | -3.00 | -3.50 | -4.00 | -4.50 | -5.00 | -5.50 | -6.00 | -6.50 | -7.00 | -7.50 | -8.00 | -8.50 | -9.00 | -9.50 | -10.00 | -10.50 |

| Code | 10000 | 10001 | 10010 | 10011 | 10100 | 10101 | 10110 | 10111 | 11000 | 11001 | 11010 | 11011 | 11100 | 11101 | 11110 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | |
| HEX | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | |
| VGL_LT/HT(V) | -11.00 | -11.50 | -12.00 | -12.50 | -13.00 | -13.50 | -14.00 | -14.50 | -15.00 | -15.50 | -16.00 | -16.50 | -17.00 | -17.50 | -18.00 | |

## VSS1 Output Set (0x07h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| | 7 | W/R | 0 | Reserve. |
| | 6 | W/R | 0 | Reserve. |
| | 5 | W/R | 0 | Reserve. |
| VSS | 4 | W/R | 0 | VSS output voltage adjustment. 0.5V/Step from -3V to -16V. Default is -6V(06h). Refer to table below. |
| | 3 | W/R | 0 | |
| | 2 | W/R | 1 | |
| | 1 | W/R | 1 | |
| | 0 | W/R | 0 | |

## VCOM1 Output Set (0x08h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| VCOM1 | 7 | W/R | 0 | VCOM_MIN+<br>(VCOM_MAX-VCOM_MIN)/127*(VCOM1[6:0])<br><br>VCOM1 = 0~127 |
| | 6 | W/R | 1 | |
| | 5 | W/R | 1 | |
| | 4 | W/R | 1 | |
| | 3 | W/R | 1 | |
| | 2 | W/R | 1 | |
| | 1 | W/R | 1 | |
| | 0 | W/R | 0 | Reserve. |

## VCOM MAX Set (0x0Ah)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| | 7 | W/R | 0 | Reserve. |
| VCOM_MAX | 6 | W/R | 0 | (AVDD/128)*(VCOM_MAX[6:0]+1)<br>VCOM_MAX DAC = 0~127 |
| | 5 | W/R | 1 | |
| | 4 | W/R | 1 | |
| | 3 | W/R | 1 | |
| | 2 | W/R | 1 | |
| | 1 | W/R | 1 | |
| | 0 | W/R | 1 | |

## VCOM MIN Set (0x0Bh)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| | 7 | W/R | 0 | Reserve. |
| VCOM_MIN | 6 | W/R | 0 | (AVDD/128)*(VCOM_MIN[6:0])<br>VCOM_MIN DAC = 0~127 |
| | 5 | W/R | 1 | |
| | 4 | W/R | 0 | |
| | 3 | W/R | 0 | |
| | 2 | W/R | 1 | |
| | 1 | W/R | 1 | |
| | 0 | W/R | 0 | |

## Gamma Output (GMA1~14) Set (0x0Ch~0x27h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| GMA1~14 | 9 | W/R | 1 | $V_{GMAx}=(V_{AVDD}/1024)*(GMAx[9:0])$<br>GMAx DAC = 0~1023 |
| | 8 | W/R | 0 | |
| | 7 | W/R | 0 | |
| | 6 | W/R | 0 | |
| | 5 | W/R | 0 | |
| | 4 | W/R | 0 | |
| | 3 | W/R | 0 | |
| | 2 | W/R | 0 | |
| | 1 | W/R | 0 | |
| | 0 | W/R | 0 | |

## Channel On/Off Set (0x28h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| Group B_EN | 7 | W/R | 1 | Group B enable control bit<br>0: Disable 1: Enable<br><br>Group B: AVDD, HAVDD, VGH, VGL, VSS1, GMA, VCOM1, VCOM2DAC |
| VGL_EN | 6 | W/R | 1 | VGL enable control bit<br>0: Disable 1: Enable |
| VSS1_EN | 5 | W/R | 1 | VSS1 enable control bit<br>0: Disable 1: Enable |
| AVDD_EN | 4 | W/R | 1 | AVDD enable control bit<br>0: Disable 1: Enable |
| HAVDD_EN | 3 | W/R | 1 | HAVDD enable control bit<br>0: Disable 1: Enable |
| GMA_EN | 2 | W/R | 1 | GMA enable control bit<br>0: Disable 1: Enable |
| VCOM1_EN | 1 | W/R | 1 | VCOM1 enable control bit<br>0: Disable 1: Enable |
| VGH_EN | 0 | W/R | 1 | VGH enable control bit<br>0: Disable 1: Enable |

## Channel Set (0x29h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| FREQ_SEL | 7 | W/R | 0 | Frequency select<br>0: 750kHz 1: 500kHz |
| | 6 | W/R | 0 | Reserve. |
| | 5 | W/R | 0 | Reserve. |
| AVDD_NMOS _INT/EXT | 4 | W/R | 0 | AVDD NMOS internal/external select<br>0: Internal 1: External |
| VGH_TYPE | 3 | W/R | 0 | VGH structure type<br>0: Boost 1: Charge pump |
| VGL_TYPE | 2 | W/R | 0 | VGL structure type<br>0: Inverting<br>1: Charge pump |
| VGL_PUMP _SOURCE | 1 | W/R | 0 | VGL charge pump source<br>0: LXBK1 1: LX/CS |
| GMA_CH_TYPE | 0 | W/R | 0 | Gamma channel type<br>0: 14-CH (GMA1~14)<br>1: 4-CH (GMA1, GMA7, GMA 8, GMA14) |

## Delay Time Set 1 (0x2Ah)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| | 7 | W/R | 0 | Reserve. |
| | 6 | W/R | 0 | Reserve. |
| DLY1_VBK1 | 5 | W/R | 0 | Delay time for VBK1<br>(TV Mode) 00: 0ms 01: 2ms 10: 4ms 11: 6ms<br>(MNT Mode) 00: 0ms 01: 40ms 10: 80ms 11: 120ms |
| | 4 | W/R | 0 | |
| DLY2_VGL | 3 | W/R | 0 | Delay time for VGL<br>00: 0ms 01: 5ms 10: 10ms 11: 15ms |
| | 2 | W/R | 1 | |
| DLY3_VSS1 | 1 | W/R | 0 | Delay time for VSS1<br>00: 0ms 01: 2ms 10: 4ms 11: 6ms |
| | 0 | W/R | 1 | |

## Delay Time Set 2 (0x2Bh)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| | 7 | W/R | 0 | Reserve. |
| DLY4_AVDD | 6 | W/R | 0 | Delay time for AVDD<br>00: 0ms 01: 5ms 10: 10ms 11: 15ms |
| | 5 | W/R | 1 | |
| DLY5_VGL | 4 | W/R | 0 | Delay time for VGL<br>00: 0ms 01: 2ms 10: 4ms 11: 6ms |
| | 3 | W/R | 1 | |
| DLY6_VCOM | 2 | W/R | 0 | Delay time for VCOM<br>000: 0ms 001: 30ms 010: 60ms 011: 90ms<br>100: 120ms 101: 150ms 110: 180ms 111: 210ms |
| | 1 | W/R | 0 | |
| | 0 | W/R | 0 | |

## Discharge Resistor Set (0x2Ch)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| ALL_DIS_EN | 7 | W/R | 1 | All channel discharge enable control bit<br>0: Disable 1: Enable |
| BK1_DIS | 6 | W/R | 1 | VBK1 discharge resistor select<br>0: 0.16kΩ 1: 1kΩ |
| AVDD_DIS | 5 | W/R | 1 | AVDD discharge resistor select<br>0: 1.4kΩ 1: 4.7kΩ |
| VGH_DIS | 4 | W/R | 1 | VGH discharge resistor select<br>0: 1.5kΩ 1: 30kΩ |
| VGL_DIS | 3 | W/R | 1 | VGL discharge resistor select<br>0: Disable 1: 10kΩ |
| HAVDD_DIS | 2 | W/R | 1 | HAVDD discharge resistor select<br>0: Disable 1: 10kΩ |
| VCOM1_DIS | 1 | W/R | 1 | VCOM1 discharge resistor select<br>00: Disable 01: 20Ω<br>10: 1kΩ 11: 8kΩ |
| | 0 | W/R | 1 | |

## PMIC Configuration 1 (0x2Dh)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| VSS1_DIS | 7 | W/R | 1 | VSS1 discharge resistor select<br>0: Disable 1: 1.2kΩ |
| | 6 | W/R | 0 | Reserve. |
| | 5 | W/R | 0 | Reserve. |
| VCOM1_DIS_TYPE | 4 | W/R | 0 | VCOM1 discharge type<br>0: VIN_UVLO_F 1: XON discharge threshold |
| HAVDD_FB | 3 | W/R | 0 | HAVDD feedback mode select<br>0: (G7+G8)/2 1: HAVDD DAC register |
| | 2 | W/R | 0 | Reserve. |
| AVDD_SS | 1 | W/R | 0 | AVDD softstart time select<br>0: 10ms 1: 20ms |
| VGH_SS | 0 | W/R | 1 | VGH softstart time select<br>0: 3ms 1: 6ms |

## VGH & VGL_VTC1/2 (0x2Eh)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| VGH&VGL_VTC2 | 7 | W/R | 1 | VGH&VGL temperature compensation, VTC2 set.<br>0.2V/Step from -0.4V to -3.4V. Default is 3.0V(0Dh).<br>Refer to table below. |
| | 6 | W/R | 1 | |
| | 5 | W/R | 0 | |
| | 4 | W/R | 1 | |
| VGH&VGL_VTC1 | 3 | W/R | 1 | VGH&VGL temperature compensation, VTC1 set.<br>0.2V/Step from -0.4V to -3.4V. Default is 2.0V(08h).<br>Refer to table below. |
| | 2 | W/R | 0 | |
| | 1 | W/R | 0 | |
| | 0 | W/R | 0 | |

| Code | 0 | 1 | 10 | 11 | 100 | 101 | 110 | 111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| VTC2(V) | 0.40 | 0.60 | 0.80 | 1.00 | 1.20 | 1.40 | 1.60 | 1.80 | 2.00 | 2.20 | 2.40 | 2.60 | 2.80 | 3.00 | 3.20 | 3.40 |

| Code | 0 | 1 | 10 | 11 | 100 | 101 | 110 | 111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| VTC1(V) | 0.40 | 0.60 | 0.80 | 1.00 | 1.20 | 1.40 | 1.60 | 1.80 | 2.00 | 2.20 | 2.40 | 2.60 | 2.80 | 3.00 | 3.20 | 3.40 |

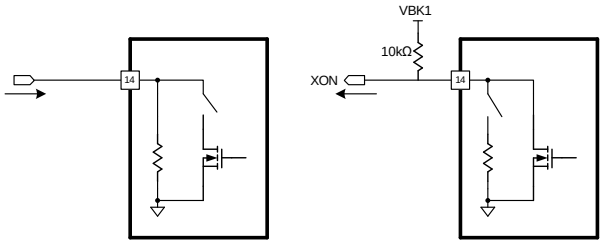
## PMIC Configuration 2 (0x30h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| | 7 | W/R | 0 | Reserve. |
| | 6 | W/R | 0 | Reserve. |
| AVDD_EXT_DRV | 5 | W/R | 0 | AVDD external driving of GATE (LX waveform 5-10ns)<br>00: EXT_DRV1_FF 01: EXT_DRV2_F<br>10: EXT_DRV3_S 11: EXT_DRV4_SS |
| | 4 | W/R | 1 | |
| VGH_Boost_COMP | 3 | W/R | 0 | VGH boost converter compensation (LX waveform 5-10ns)<br>00: VGH_COMP1_FF 01: VGH_COMP2_F<br>10: VGH_COMP3_S 11: VGH_COMP4_SS |
| | 2 | W/R | 0 | |
| VGL_Inverting _COMP | 1 | W/R | 0 | VGL inverting compensation (LX waveform 5-10ns)<br>00: VGL_COMP1_FF 01: VGL_COMP2_F<br>10: VGHL_COMP3_S 11: VGL_COMP4_SS |
| | 0 | W/R | 1 | |

## PMIC Configuration 3 (0x31h)

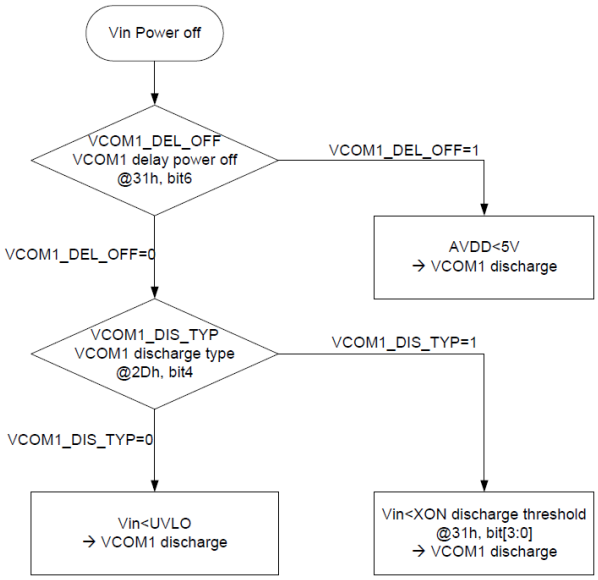
| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| EN_PIN_SEL | 7 | W/R | 0 | EN pin function select.<br>0: EN input function 1: XON output function |
| VCOM1_DLY_OFF | 6 | W/R | 0 | VCOM1 delay power off.<br>0: Disable 1: Enable |
| HAVDD_DLY_OFF | 5 | W/R | 0 | HAVDD delay power off.<br>0: Disable 1: Enable |
| GMA_DLY_OFF | 4 | W/R | 0 | Gamma 1~14 delay power off.<br>0: Disable 1: Enable |
| XON_DIS_THR | 3 | W/R | 0 | XON discharge threshold.<br>(TV mode) 0.25V/Step from 6.5V to 10.25V. Default is 7.0V(02h).<br>(MNT mode) 0.14V/Step from 3.63V to VINUV. Default is 3.77V(02h).<br>Refer to table below. |
| | 2 | W/R | 0 | |
| | 1 | W/R | 1 | |
| | 0 | W/R | 0 | |

## EN_PIN_SEL




Bit7=0, EN function  Bit7=1, XON function

## VCOM1_DLY_OFF




## XON_DIS_THR

| Code | 0 | 1 | 10 | 11 | 100 | 101 | 110 | 111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| XON(V) | 6.50 | 6.75 | 7.00 | 7.25 | 7.50 | 7.75 | 8.00 | 8.25 | 8.50 | 8.75 | 9.00 | 9.25 | 9.50 | 9.75 | 10.00 | 10.25 |

| Code | 0 | 1 | 10 | 11 | 100 | 101 | 110 | 111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DEC | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| HEX | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| XON(V) | 3.63 | 3.77 | 3.91 | 4.05 | 4.19 | 4.33 | 4.47 | 4.60 | 4.74 | 4.88 | 5.02 | 5.16 | 5.30 | 5.44 | 5.58 | VINUV |

## VCOM2DAC Set (0x45h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| VCOM2DAC | 7 | W/R | 0 | VCOM_MIN+ (VCOM_MAX-VCOM_MIN)/127*(VCOM2DAC[6:0])<br>VCOM2DAC = 0~127 |
| | 6 | W/R | 1 | |
| | 5 | W/R | 1 | |
| | 4 | W/R | 1 | |
| | 3 | W/R | 1 | |
| | 2 | W/R | 1 | |
| | 1 | W/R | 1 | |
| | 0 | W/R | 0 | Reserve. |

## PMIC Configuration 4 (0x46h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| MNT_MODE_EN | 7 | W/R | 0 | MNT Mode select.<br>0: TV mode 1: MNT mode |
| | 6 | W/R | 0 | |
| | 5 | W/R | 0 | |
| | 4 | W/R | 0 | |
| | 3 | W/R | 0 | |
| | 2 | W/R | 0 | |
| | 1 | W/R | 0 | |
| VCOM2DAC_EN | 0 | W/R | 1 | VCOM2DAC control bit<br>0: Disable 1: Enable |

## EEPROM Control (0xFFh)

The NVM will be written to or read from through the Control Register. The control register is a register only (cannot be written into NVM)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| W_ALL | 7 | W/R | 0 | 1: Write all data from DAC register to EEPROM |
| W_VCOM1 | 6 | W/R | 0 | 1: Write VCOM1 data from DAC register to EEPROM |
| | 5 | W/R | 0 | Reserve. |
| | 4 | W/R | 0 | Reserve. |
| | 3 | W/R | 0 | Reserve. |
| | 2 | W/R | 0 | Reserve. |
| | 1 | W/R | 0 | Reserve. |
| EE/DR | 0 | W/R | 0 | 0: Read data from DAC register.<br>1: Read data from EEPROM |

# Slaver Address (0xE8h)

## VCOM1 Configuration 1 (0x00h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| | 7 | W/R | 0 | Reserve. |
| | 6 | W/R | 0 | Reserve. |
| | 5 | W/R | 0 | Reserve. |
| RESET | 4 | W/R | 0 | Down load VCOM1 data from EEPROM to DAC register.<br>0: Disable 1: Enable |
| VCOM1_WR_EPM | 3 | W/R | 0 | Write VCOM1 data from DAC register to EEPROM.<br>0: Disable 1: Enable |
| | 2 | W/R | 0 | Reserve. |
| OUT_EN | 1 | W/R | 1 | VCOM1 output control bit.<br>0: Disable (VCOM1 output Hi-Z) 1: Enable |
| | 0 | W/R | 0 | Reserve. |

## VCOM1 Output Set (0x01h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| VCOM1 | 7 | W/R | 0 | VCOM_MIN+<br>(VCOM_MAX-VCOM_MIN)/127*(VCOM1[6:0])<br><br>VCOM1 = 0~127 |
| | 6 | W/R | 1 | |
| | 5 | W/R | 1 | |
| | 4 | W/R | 1 | |
| | 3 | W/R | 1 | |
| | 2 | W/R | 1 | |
| | 1 | W/R | 1 | |
| | 0 | W/R | 0 | Reserve. |

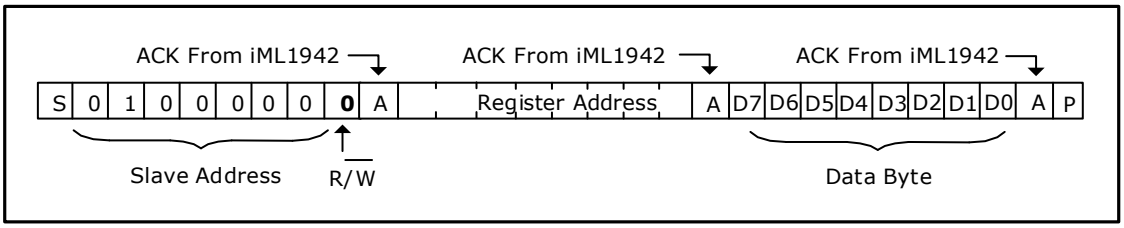
## FAULT Flag (0x02h)

| Name | # of Bits | Access | Default | Description |
|---|---|---|---|---|
| OTP | 7 | R | 0 | 0: Disable 1: Enable<br>Release IC restart. |
| LS NG | 6 | R | 0 | 0: Disable 1: Enable<br>Release IC restart. |
| VBK1 UVP or SCP | 5 | R | 0 | 0: Disable 1: Enable<br>Release IC restart. |
| AVDD UVP or SCP | 4 | R | 0 | 0: Disable 1: Enable<br>Release IC restart. |
| VGH UVP or SCP | 3 | R | 0 | 0: Disable 1: Enable<br>Release IC restart. |
| VGL UVP or SCP | 2 | R | 0 | 0: Disable 1: Enable<br>Release IC restart. |
| VSS1 UVP | 1 | R | 0 | 0: Disable 1: Enable<br>Release IC restart. |
| HAVDD UVP or SCP | 0 | R | 0 | 0: Disable 1: Enable<br>Release IC restart. |

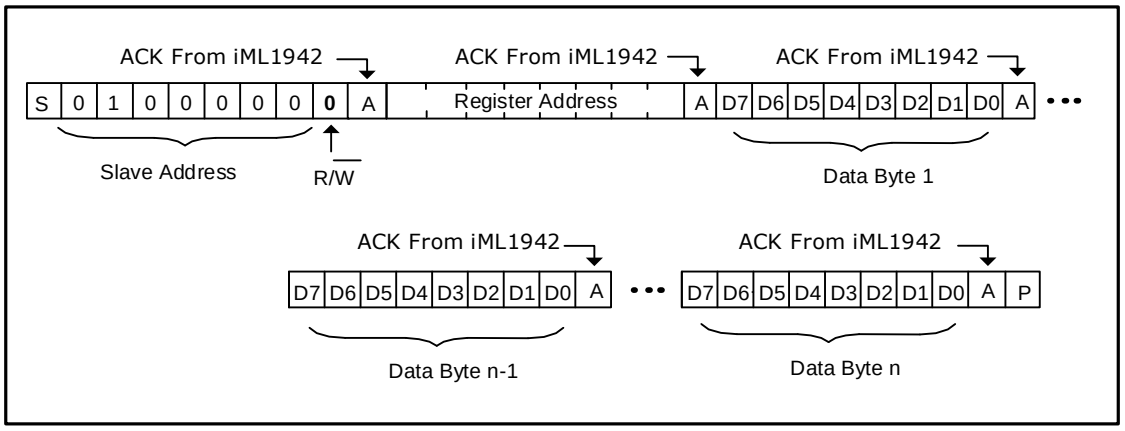
# I²C Interface Protocol

*Write Operation (Slaver Address 0x40h)*

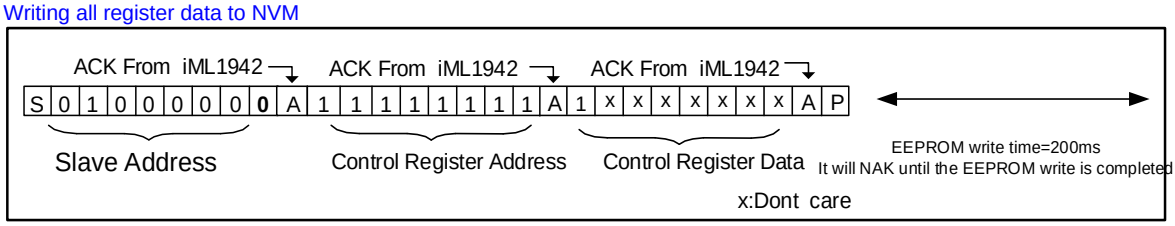
Writing to a single DAC register




Writing to multiple DAC registers

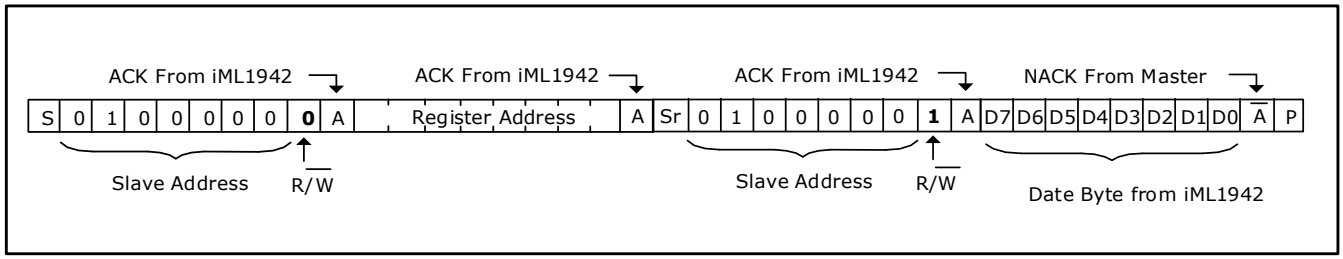



Writing all register data to NVM

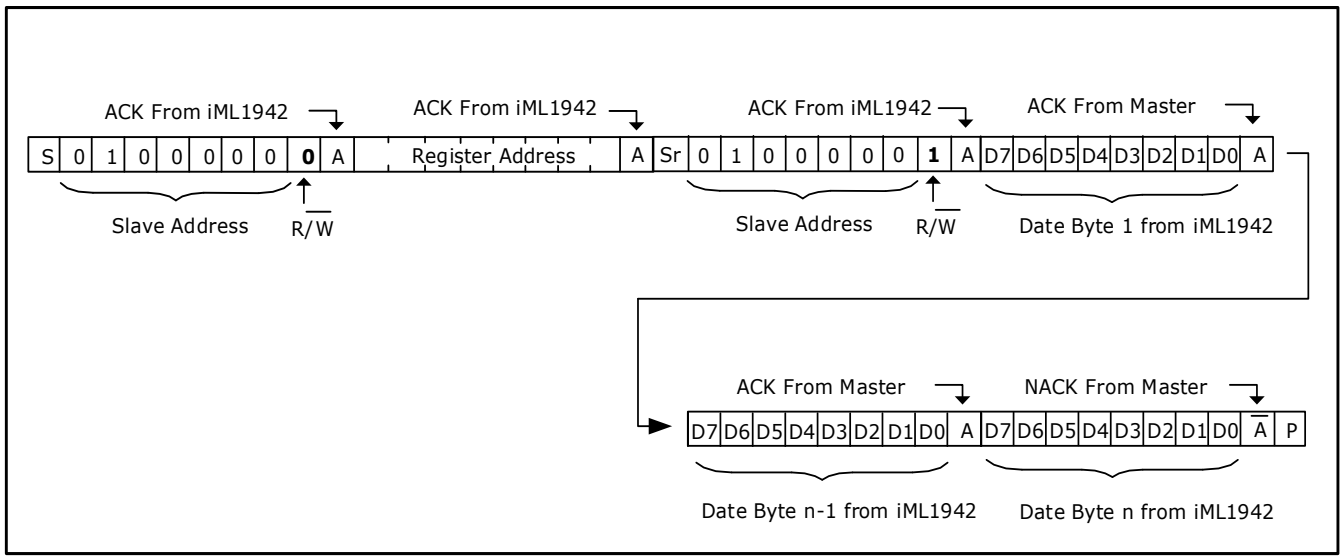


*Read Operation (Slaver Address 0x40h)*

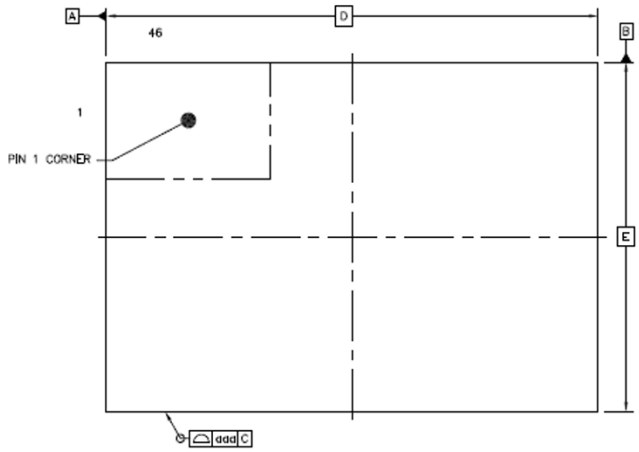
Reading from a single DAC register



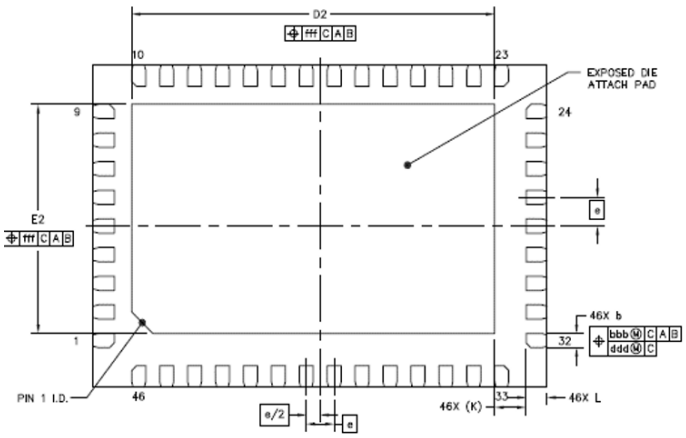

Reading from a Multiple DAC register



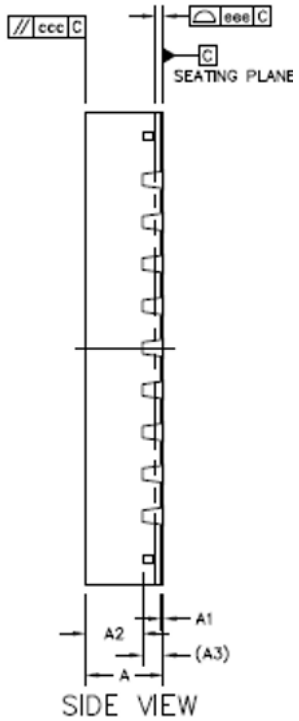
# PACKAGE INFORMATION-WQFN 6.5x4.5mm-46PIN




TOP VIEW



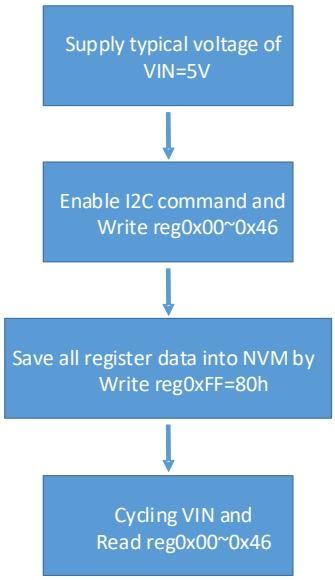

BOTTOM VIEW

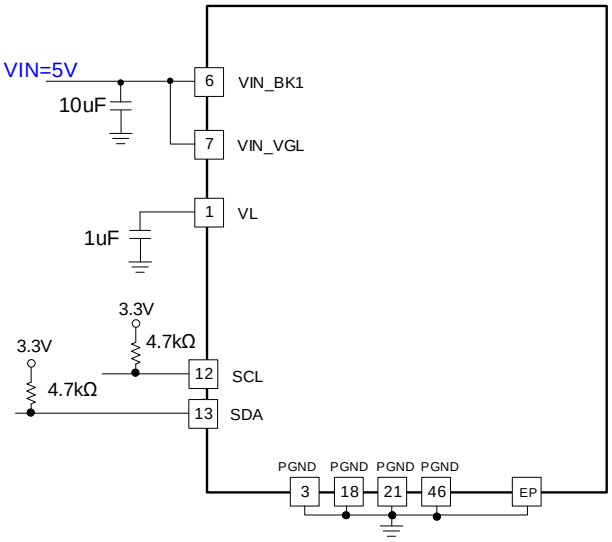



SIDE VIEW

| Symbol | Chipone | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.203 REF | |
| b | 0.15 | 0.20 | 0.25 |
| D | 6.40 | 6.50 | 6.60 |
| D2 | 5.10 | 5.20 | 5.30 |
| E | 4.40 | 4.50 | 4.60 |
| E2 | 3.10 | 3.20 | 3.30 |
| e | | 0.40 REF | |
| L | 0.20 | 0.30 | 0.40 |
| K | | 0.45 REF | |
| aaa | | 0.10 | |
| ccc | | 0.10 | |
| eee | | 0.08 | |
| bbb | | 0.07 | |
| ddd | | 0.05 | |
| fff | | 0.10 | |
| N | | 46 | |

# IC PROGRAMMER DIAGRAM



# LAND PATTERN FOR WQFN-6.5X4.5MM PACKAGE