Blue LED Local Dimming Light Module

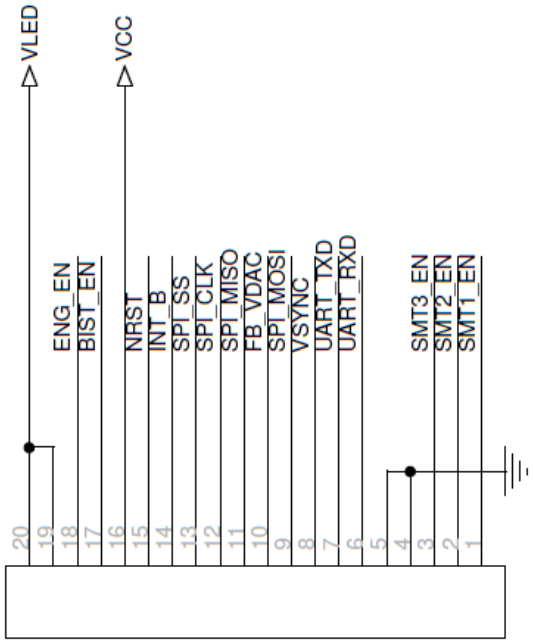
1. Features

- **Supply Voltage**
  VCC 2.7V ~ 3.6V
- **Flexible BLU Sizing Support**
  Max. Tx Port No.: 2
- **Support Hybrid LED Driving Scheme**
  PM (Scan Mode)
  AM (Direct Driving)
- **Programmable Tx Port Output Skew Control**
  Dedicated Setting for Each Tx Port
- **VSYNC Support**
  Direct Driving Mode: 60 ~ 240Hz
- **SPI Interface**
  Max Speed: 16MHz
- **VLED Adjustable (FB_VDAC)**
  VDAC Output Range: 0.2V ~ AVDD-0.2V
  Resolution: 12-bit
- **Light Plate Diagnosis (INT_B):**
  Addressing Failure
  Over Temperature Assertion
  LED Open/Short Occurrence
  Checksum Error for SPI I/F
- **BIST Function (BIST_EN):**
- **Driving current range, (0.5~5mA), (1.0~10mA), (2.0~20mA) and (3.0~30mA)**
- **Individual 7 bit I-DAC for each I-sink**
- **0.4V saturation voltage @25mA for each I- sink**
- **12-Bit true brightness control resolution with PWM dimming at 3840Hz (without dither)**
- **PWM output frequency support (direct driving mode): 60/120/144/240/480/960/1920/3840 Hz**
- **PWM output frequency accuracy: +/-2%**
- **DC I-sink accuracy: +/-2%**
- **Dimming mode control scheme**
  -PWM - 12 bits
- **Local dimming zone: 56 zones**
- **Light module thickness < 0.4mm**

2. Application

- **LED FALD backlight system**

3. Pin Outline (TOP VIEW)

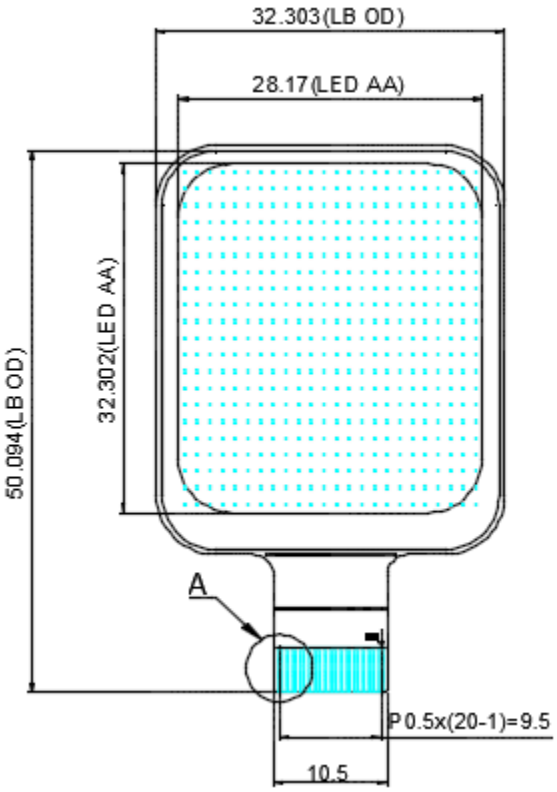


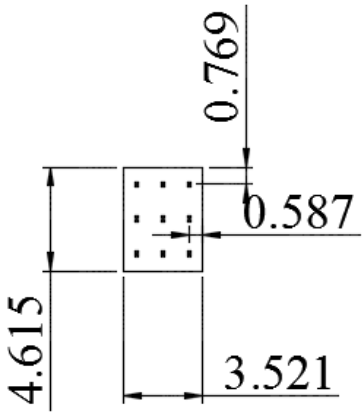
4.Pin Description

I: Input, **O**: Output, **I/O**: both Input and Output, **AI**: Analog Input, **AO**: Analog Output, **P**: Power

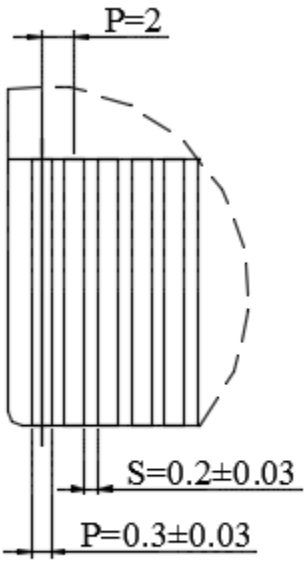
Pin Name	Type	Description
BIST_EN	**I**	BIST mode enable
VLED	**I**	3.3V Power Supply
VSS	**Ground**	Ground
VCC	**Power**	3.3V Power Supply
NRST	**I**	Reset control, low active
INT_B	**OD**	Interrupt indicator, active low
SPI_SS	**I**	Chip select
SPI_CLK	**I**	Clock
SPI_MISO	**I**	Master input pin from slave
FB_VDAC	**AO**	DAC output for VLED control
SPI_MOSI	**O**	Master output to slave
VSYNC	**I**	Frame synchronization
UART_Tx	**I**	Tx port for UART
UART_Rx	**I/O**	Rx port for UART
VSS	**Ground**	Ground
SMT_EN3	**I**	Test Mode 3
SMT_EN2	**I**	Test Mode 2
SMT_EN1	**I**	Test Mode 1
ENG_En	**I**	Engineering mode enable

5.Light module dimensions





Single Zone Dimension



Detail A

1. General Tolerance : ±0.2mm
2. FPC Pad Tolerance : ±0.02mm
3. OC T=0.25mm

6. Absolute Maximum Ratings

Description	Spec
DC Power Supply, V_{DD}-V_{SS}	-0.3V to 4V
Variations between different power pins, V_{DDx} - V_{DD}	50mV
Allowed voltage difference for V_{DD} and AV_{DD}, V_{DD} - AV_{DD}	50mV
Variations between different ground pins, V_{SSx} - V_{SS}	50mV
Allowed voltage difference for V_{SS} and AV_{SS}, V_{SS} - AV_{SS}	50mV
Maximum current into V_{DD}	150mA
Maximum current out of V_{SS}	100mA
Maximum current sunk by a I/O Pin	20mA
Maximum current sourced by a I/O Pin	20mA
Operating ambient temperature range	-40°C to 105°C
Operating junction temperature range	-40°C to 125°C
Storage temperature range	-65°C to 150°C
ESD, Human Body Model (HBM)	2kV
ESD, Charge Device Model (CDM)	200V
Latch-Up	400mA

7. Optical-Electrical Specifications

(V_{DD}=3.3V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
System Supply						
Input Supply Voltage	V_{DD} = AV_{DD}		2.7		3.6	V
Active Current	I_{DD}	Normal Operation @72MHz	-	-	24	mA
Suspend Current	I_{DDS}	BL_En = 1, PWD_En = 1		3.5		mA
Power Down Current	I_{PD}	BL_En = 0		1.7		mA
IO Voltage Level						
Logic Input Low Level	VIL		0	-	0.3 V_{DD}	V
Logic Input High Level	VIH		0.7 V_{DD}	-	V_{DD}	
Hysteresis Voltage	Vhy			0.2 V_{DD}		V
Input Leakage Current			-1		1	uA
Pull up Resistor	R_{PU}	VDD=3.6V		38		kΩ
Source Current	I_{Sour}	VDD=3.3V, Vin=(V_{DD}-0.4V)		10		mA
Sink Current	I_{Sink}	VDD=3.3V, Vin=0.4V		9		mA

I/O pin capacitance	Cio			5		pF
NRST pin filtered time	tFR1			32		uS
Blue LED light module						
LED Active Area				X=28.170 Y=32.302		mm
Luminous Intensity	Po	ILED=2mA		2016		mw
LED Pitch_X	LED_Px	Center to Center		1.1735		mm
LED Pitch_Y	LED_Py	Center to Center		1.5380		mm
Light Module Thickness	t			0.4		mm
Local Dimming Zone				56		zone
LED Count. Per Zone				9		ea
Single Zone Dimension				X=3.521 Y=4.615		mm
Dominant Wavelength	λ			450		nm

8.SPI Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Units
SPI SLAVE MODE (VDD = 2.7~3.6V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]			T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]			T_{SPICLK} / 2	ns
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns
t_{DS}	Data input setup time	1.5	-	-	ns
t_{DH}	Data input hold time	3.5	-	-	ns
t_V	Data output valid time	-	-	17.5	ns
Note: 1. The minimum clock period for SPICLK is 62.5 ns (16 MHz).