CJC1808

Analog-Input 24-Bit Stereo ADC

Data Sheet

Version	author	data	description
V1.0	By tf	2016.12	The first draft
V1.1	By tf	2018.1	

Contents

1. General Discription

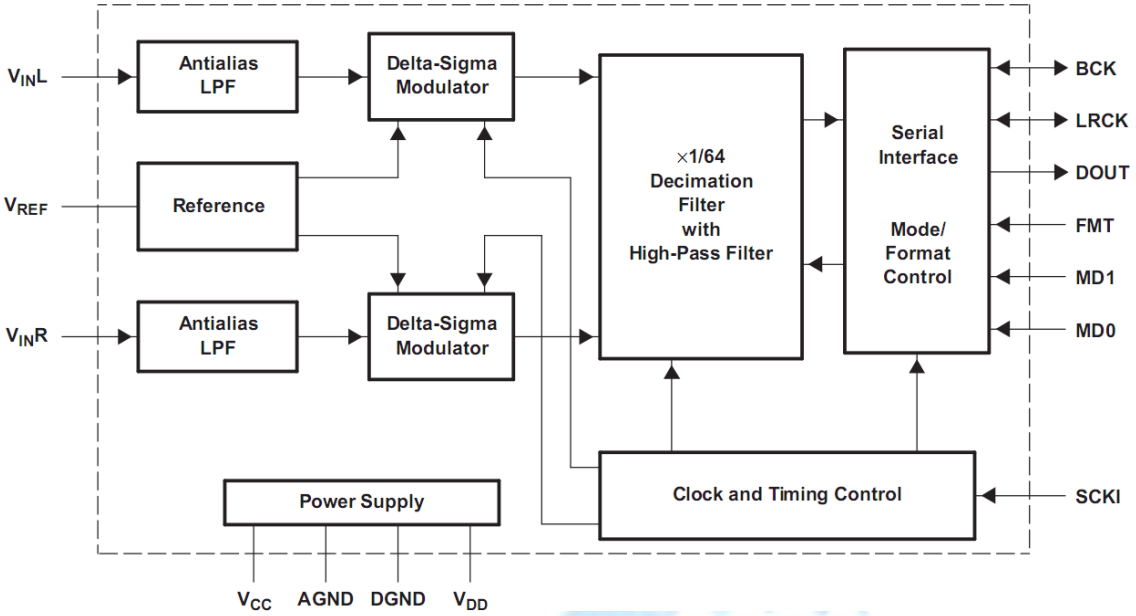
The CJC1808 device is a high-performance, low-cost, single-chip, stereo analog-to-digital converter with single-ended analog voltage input. The CJC1808 device uses a delta-sigma modulator with 64-times oversampling and includes a digital decimation filter and high-pass filter that removes the dc component of the input signal. For various applications, the CJC1808 device supports master and slave mode and two data formats in serial audio interface.

Fabrication of the CJC1808 device uses a highly advanced CMOS process. The device is available in a small, 14-pin TSSOP package.

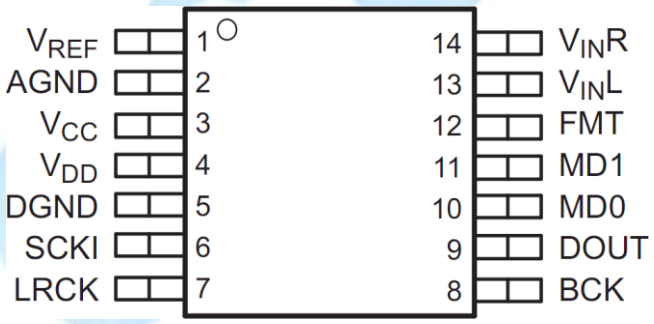
2. Features

- ☐ Stereo Δ-Σ ADC
- ☐ On-chip digital anti-alias filter
- ☐ Single-ended input
- ☐ Digital high-pass filter to eliminate DC offset
- ☐ S/(N+D): 87dB@3.3V for 48kHz
- ☐ DR: 101dB@3.3V for 48kHz
  99dB@3.3V for 96kHz
- ☐ S/N: 101dB@3.3V for 48kHz
  99dB@3.3V for 96kHz
- ☐ Sampling Rate: 8kHz ～ 96kHz
- ☐ System Clock:
  256fs/384fs/512fs
- ☐ CMOS Input Level
- ☐ Master/Slave mode
- ☐ Audio Interface: Left-justified, 24-bit/I2S, 24-bit
- ☐ Power Supply: 2.7 to5.5V
- ☐ Ta= —40~85℃（industrial）, Ta=—20~85℃（commercial）
- ☐ Package:14-pin TSSOP

3. Diagram



4. Pin Layout



5. Pin/Function

NO.	Pin Name	I/O	Function
1	VREF	-	Reference-voltage decoupling (1/2VCC)
2	AGND	-	Analog GND
3	VCC	-	Analog power supply, 3.3-V
4	VDD	-	Digital power supply, 3.3-V
5	DGND	-	Digital GND
6	SCKI	I	System clock input; 256 fS, 384 fS or 512 fS
7	LRCK	I/O	Audio-data latch-enable input or output
8	BCK	I/O	Audio-data bit-clock input or output
9	DOUT	O	Audio-data digital output
10	MD0	I	Audio-interface mode select 0
11	MD1	I	Audio-interface mode select 1
12	FMT	I	Audio-interface format select "L": I^2S ,24bit Compatible , "H": Left-justified, 24-bit
13	VINL	I	Analog input, L-channel
14	VINR	I	Analog input, R-channel

6. Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range

			MIN	MAX	UNIT
VCC	Analog supply voltage		–0.3	5.5	V
VDD	Digital supply voltage		–0.3	4	V
	Ground voltage differences	AGND, DGND		±0.1	V
	Digital input voltage	LRCK, BCK, DOUT	–0.3	(VDD+0.3 V)<4	V
		SCKI, MD0, MD1, FMT	–0.3	5.5	V
VINL,VINR, VREF	Analog input voltage		–0.3	(VCC+0.3 V)<5.5	V
	Input current (any pins except supplies)			±10	mA
TJ	Junction temperature			150	°C
Tstg	Storage temperature		–55	150	°C

6.2 Recommended Operating Conditions

over operating ambient temperature range

		MIN	NOM	MAX	UNIT
VCC	Analog supply voltage	2.7	3.3	5.5	V
VDD	Digital supply voltage	2.7	3.3	3.6	V
	Analog input voltage, full scale (–0 dB)		1.98		Vpp
VIH	High input logic level	2		VDD	V
VIL	Low input logic level	0		0.8	V
	Digital input logic family		TTL compatible		
	Digital input clock frequency, system clock	2.048		49.152	MHz
	Digital input clock frequency, sampling clock	8		96	kHz
	Digital output load capacitance			20	pF
TA	Operating ambient temperature range			150	°C
TJ	Junction temperature	–55		150	°C

6.3 Electrical Characteristics

All specifications at TA = 25°C, VCC = 3.3 V, VDD = 3.3 V, master mode, fS = 48 kHz, system clock = 512 fS, 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Resolution			24		Bits
DATA FORMAT						
	Audio data interface format			I2S, left-justified		
	Audio data bit length			24		Bits
	Audio data format			MSB-first, 2s complement		
fs	Sampling frequency		8	48	96	kHz
	System clock frequency	256 fs	2.048	12.288	24.576	MHz
		384 fs	3.072	18.432	36.864	
		512 fs	4.096	24.576	49.152	
INPUT LOGIC						
VIH	High input logic level		2		VDD	V
VIL	Low input logic level		0		0.8	V
IIH	High input logic current		±10			µA
IIL	Low input logic current		±10			µA
OUTPUT LOGIC						
VOH	High output logic level	IOUT = –4 mA			2.8	V
VOL	Low output logic level	IOUT = 4 mA			0.5	V

6.4 Electrical Characteristics(continued)

All specifications at TA = 25°C, VCC = 3.3 V, VDD = 3.3 V, master mode, fS = 48 kHz, system clock = 512 fS, 24-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN NOM MAX	UNIT
DYNAMIC PERFORMANCE				
THD+N	Total harmonic distortion + noise	VIN = –0 dB, fs = 48 kHz	-83	dB
		VIN = –0 dB, fs = 96 kHz	-81	
		VIN = –60 dB, fs = 48 kHz	-32	
		VIN = –60 dB, fs = 96 kHz	-31	
	Dynamic range	fs = 48 kHz, A-weighted	91	dB
		fs = 96 kHz, A-weighted	87	
S/N	Signal-to-noise ratio	fs = 48 kHz, A-weighted	91	dB
		fs = 96 kHz, A-weighted	87	
	Channel separation	fs = 48 kHz	92	
		fs = 96 kHz	92	
ANALOG INPUT				
	Input voltage		0.6 VCC	Vpp
	Center voltage (VREF)		0.5 VCC	V
	Input impedance			kΩ
DIGITAL FILTER PERFORMANCE				
	Pass band		0.49fs	Hz
	Stop band		0.57fs	Hz
	Pass-band ripple		±0.035	dB
	Stop-band attenuation		-70	dB
POWER SUPPLY REQUIREMENTS				
ICC	Analog supply current	fs = 48 kHz	15.1	mA
		Powered down	0.8	mA
IDD	Digital supply current	fs = 48 kHz	1.38	mA
		Powered down	0.1	mA

6.5 Timing Requirements

		MIN	NOM	MAX	UNIT
SYSTEM CLOCK TIMING					
tw(SCKH)	System clock pulse duration, HIGH		8		ns
tw(SCKL)	System clock pulse duration, LOW		8		ns
	System clock duty cycle	45		55	%
CLOCK-HALT POWER-DOWN AND RESET TIMING					
t(CKR)	Delay time from SCKI halt to internal reset	4			µs
t(RST)	Delay time from SCKI resume to reset release			1024 SCKI	µs
t(REL)	Delay time from reset release to DOUT output			8960 / fs	µs
AUDIO DATA INTERFACE TIMING (Slave Mode: LRCK and BCK Work as Inputs)(1)					
t(BCKP)	BCK period	1 / (64 f)			ns
t(BCKH)	BCK pulse duration, HIGH	1.5 × t(SCKI)			ns
t(BCKL)	BCK pulse duration, LOW	1.5 × t(SCKI)			ns
t(LRSU)	LRCK setup time to BCK rising edge	50			ns
t(LRHD)	LRCK hold time to BCK rising edge	10			ns
t(LRCP)	LRCH period	10			us
t(CKDO)	Delay time, BCK falling edge to DOUT valid	-10		40	ns
t(LRDO)	Delay time, LRCK edge to DOUT valid	-10		40	ns
tr	Rise time of all signals			20	ns
tf	Fall time of all signals			20	ns
AUDIO DATA INTERFACE TIMING (Master Mode: LRCK and BCK Work as Outputs)(2)					
t(BCKP)	BCK period	150	1 / (64 fs)	2000	ns
t(BCKH)	BCK pulse duration, HIGH	65		1200	ns
t(BCKL)	BCK pulse duration, LOW	65		1200	ns
t(CKLR)	Delay time, BCK falling edge to LRCK valid	-10		20	ns
t(LRCP)	LRCK period	10	1 / fs	125	ns
t(CKDO)	Delay time, BCK falling edge to DOUT valid	-10		20	ns
t(LRDO)	Delay time, LRCK edge to DOUT valid	-10		20	ns
tr	Rise time of all signals			20	ns
tf	Fall time of all signals			20	ns
AUDIO CLOCK INTERFACE TIMING (Master Mode: BCK Work as Outputs)(3)					
t(SCKBCK)	Delay time, SCKI rising edge to BCK edge	5		30	ns

(1) Timing measurement reference level is 1.4 V for input and 0.5 VDD for output. Rise and fall times are from 10% to 90% of the input-output signal swing. Load capacitance of DOUT is 20 pF. t(SCKI) is the SCKI period.

(2) Timing measurement reference level is 0.5 VDD. Rise and fall times are from 10% to 90% of the input-output signal swing. Load capacitance of all signals is 20 pF.

(3) Timing measurement reference level is 1.4 V for input and 0.5 VDD for output. Load capacitance of BCK is 20 pF. This timing applies when SCKI frequency is less than 25 MHz.

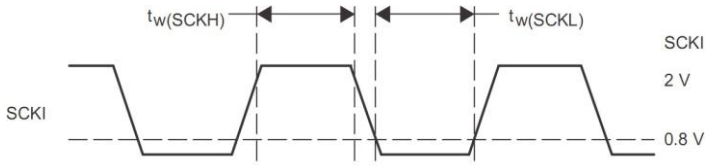


Figure 1. System Clock Timing

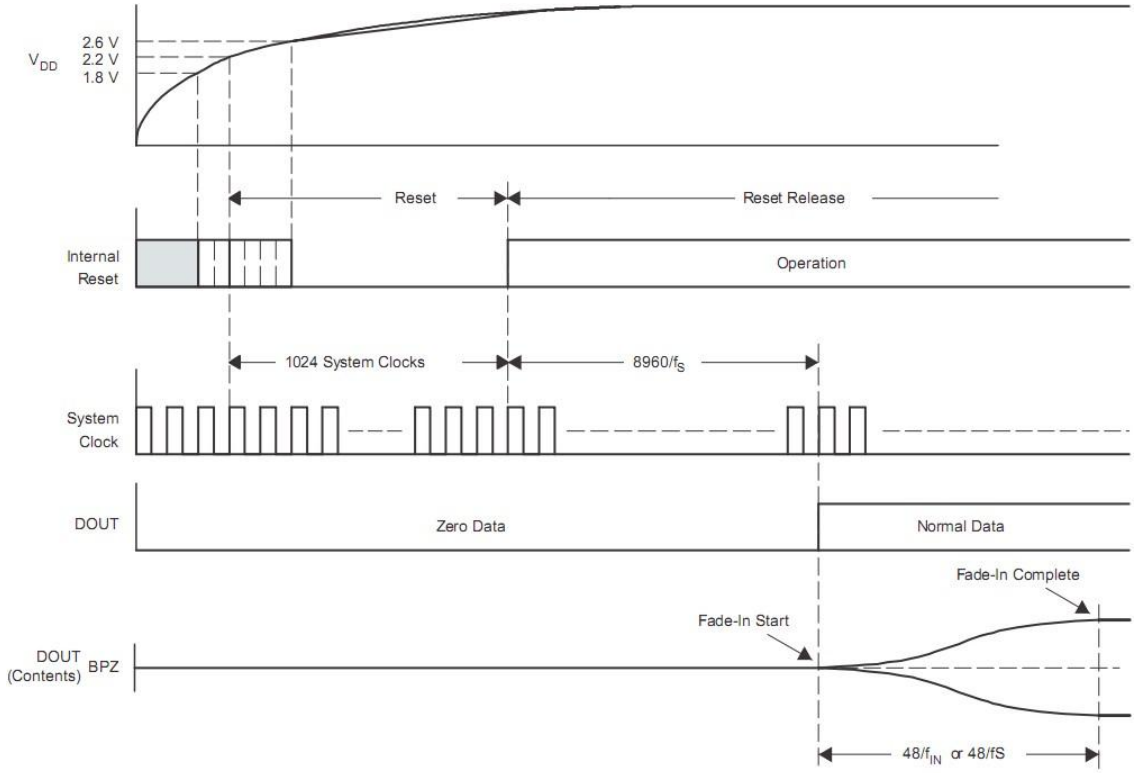


Figure 2. Power-On Timing

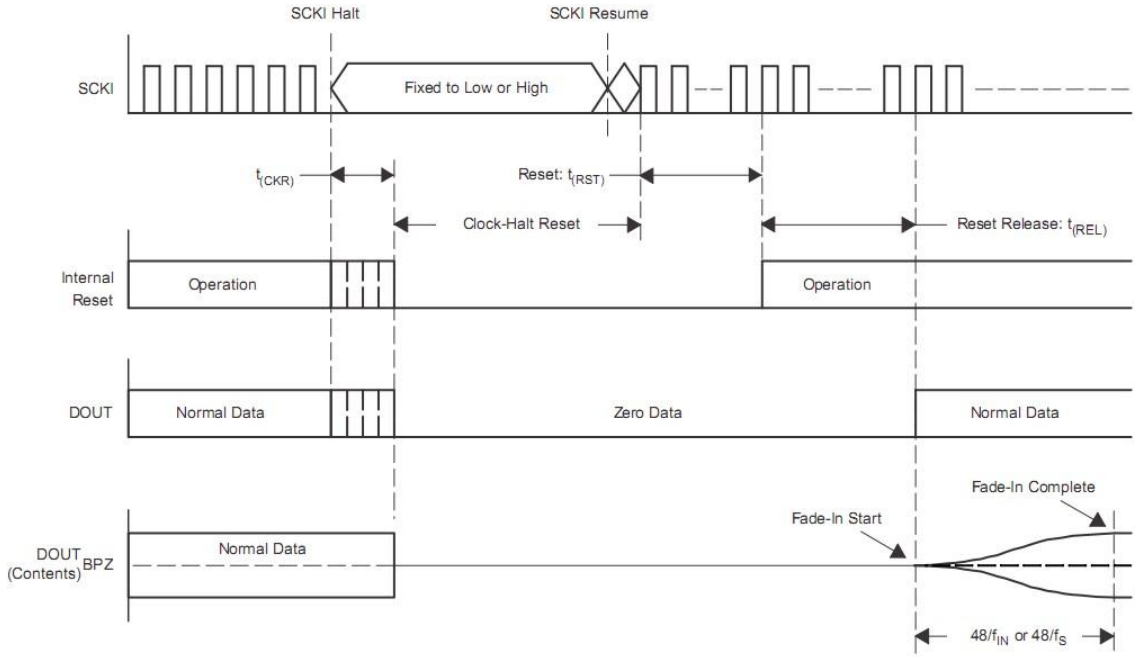


Figure 3. Clock-Halt Power-Down and Reset Timing

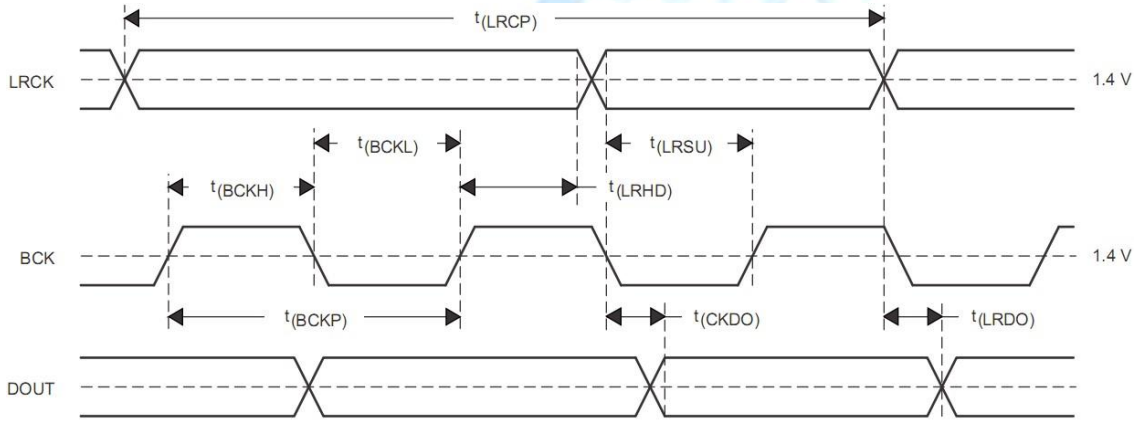


Figure 4. Audio Data Interface Timing (Slave Mode: LRCK and BCK Work as Inputs)

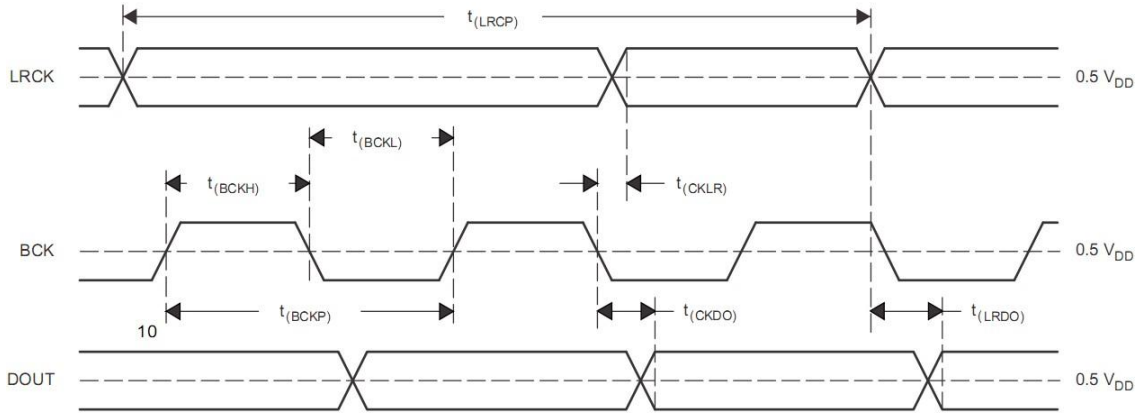


Figure 5. Audio Data Interface Timing (Master Mode: LRCK and BCK Work as Outputs)

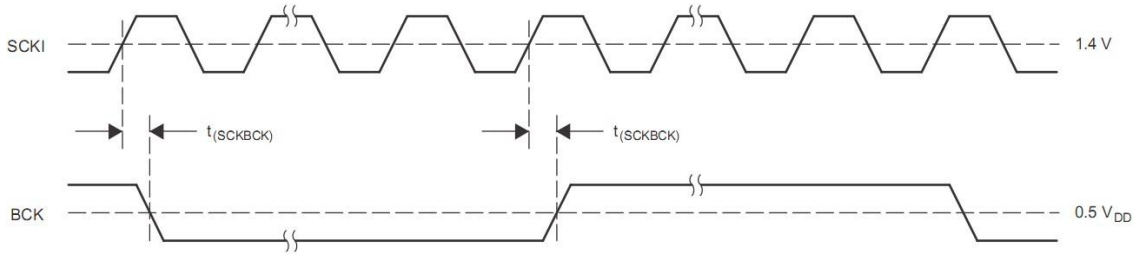


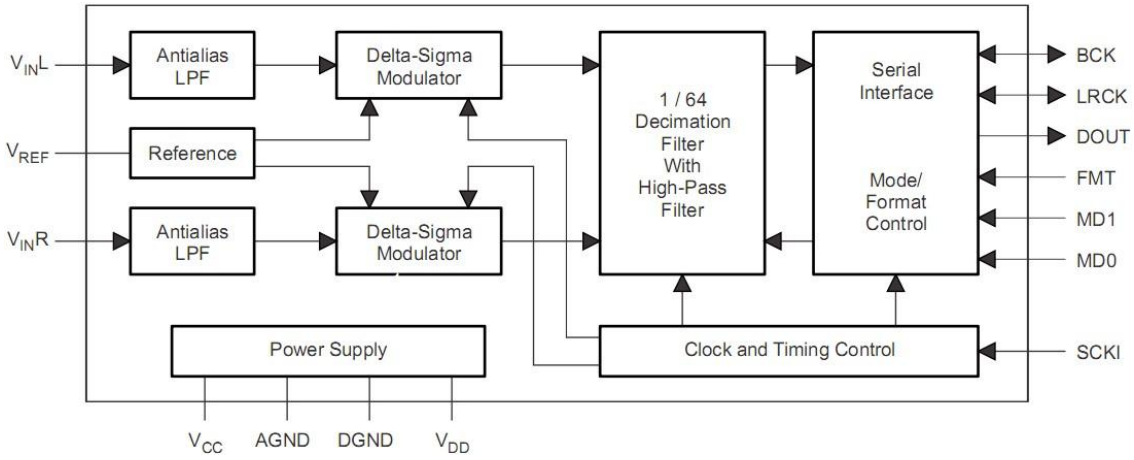
Figure 6. Audio Clock Interface Timing (Master Mode: BCK Works as Output)

7. Detailed Description

7.1 Overview

The CJC1808 is high-performance, low-cost, single-chip, stereo analog-to-digital converter with single-ended analog voltage input. The CJC1808 uses a delta-sigma modulator with 64-times oversampling and includes a digital decimation filter and high-pass filter that removes the dc component of the input signal. For various applications, the CJC1808 supports master and slave mode and two data formats in serial audio interface up to 96-kHz sampling. These features are controlled through hardware by pulling pins high or low with resistors or a controller GPIO. The CJC1808 also supports a power-down and reset function by means of halting the system clock.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Hardware Control

Pins FMT, MD0, and MD1 allow the device to be controlled by either pullup or pulldown resistors as well as GPIO from a digital IC. These controls allow the option of switching between I2S or left-justified, and in which interface mode the device operates.

7.3.2 System Clock

The CJC1808 device supports 256 fS, 384 fS, and 512 fS as system clock, where fS is the audio sampling frequency. The system clock input must be on SCKI (pin 6).

The CJC1808 device has a system-clock detection circuit which automatically senses if the system-clock operation is at 256 fS, 384 fS, or 512 fS in slave mode. In master mode, control of the system clock frequency must be through the serial control port, which uses MD1 (pin 11) and MD0 (pin 10). An internal circuit automatically divides down the system clock to generate frequencies of 128 fS and 64 fS, which operate the digital filter and the delta-sigma modulator, respectively.

Table 1 shows some typical relationships between sampling frequency and system clock frequency, and Figure 1 shows system clock timing.

SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (f) (MHz)		
	256 fs	384 fs	512 fs
8	2.048	3.072	4.096
16	4.096	6.144	8.192
32	8.192	12.288	16.384
44.1	11.2986	16.9344	22.5792
48	12.288	18.432	24.576
64	16.384	24.576	32.768
88.2	22.5792	33.8688	45.1584
96	24.576	36.864	49.152

Table 1. Sampling Frequency and System Clock Frequency (continued)

7.3.3 Synchronization With Digital Audio System

In slave mode, the CJC1808 device operates under LRCK (pin 7), synchronized with system clock SCKI (pin 6).

The CJC1808 device does not require a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCKs for 64 BCK/frame (±5 BCKs for 48 BCK/frame) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within 1 / fs and digital output goes to zero data (BPZ code) until resynchronization between LRCK and SCKI occurs.

In the case of changes less than ±5 BCKs for 64 BCK/frame (±4 BCKs for 48 BCK/frame), resynchronization does not occur, and the previously described digital output control and discontinuity do not occur.

Figure 23 illustrates the digital output response for loss of synchronization and resynchronization. During undefined data, the CJC1808 device can generate some noise in the audio signal. Also, the transition of normal data to undefined data creates a discontinuity in the digital output data, which can generate some noise in the audio signal. The digital output is valid after resynchronization completes and the time of 32 / fs has elapsed. Because the fade-in operation is performed, it takes additional time of 48 / fin or 48 / fs to obtain the level corresponding to the analog input signal. In the case of loss of synchronization during the fade-in or fade-out operation, the operation stops and DOUT (pin 9) goes to zero data immediately. The fade-in operation resumes from mute after the time of 32 / fs following resynchronization.

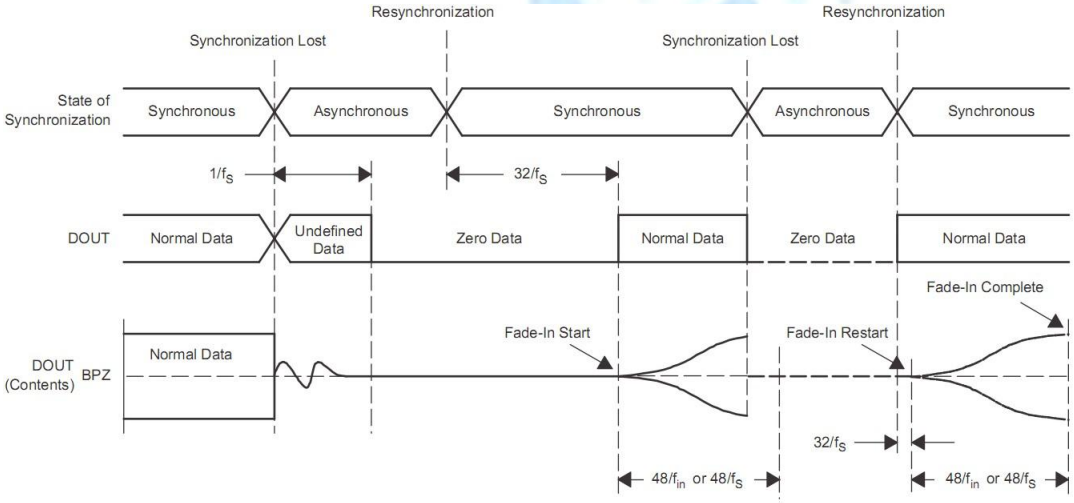


Figure 23. ADC Digital Output for Loss of Synchronization and Resynchronization

7.3.4 Power On

The CJC1808 device has an internal power-on-reset circuit, and initialization (reset) occurs automatically when the power supply (VDD) exceeds 2.2 V (typical). While VDD < 2.2 V (typical), and for 1024 system-clock counts after VDD > 2.2 V (typical), the CJC1808 device stays in the reset state and the digital output remains zero. After release of the reset state, 8960 / fs seconds must pass before the digital output becomes valid. Because of the performing of the fade-in operation, it takes additional time of 48 / fin or 48 / fs to obtain the data corresponding to the analog input signal. Figure 2 illustrates the power-on timing and the digital output.

7.3.5 Serial Audio Data Interface

The CJC1808 device interfaces the audio system through LRCK (pin 7), BCK (pin 8), and DOUT (pin 9).

7.3.5.1 Interface Mode

MD1 (pin 11) and MD0 (pin 10) select master mode and slave mode as interface modes, both of which the CJC1808 device supports.Table 2 shows the interface-mode selections. It is necessary to set MD1 and MD0 prior to power on.

In master mode, the CJC1808 device provides the timing of serial audio data communications between the CJC1808 device and the digital audio processor or external circuit. While in slave mode, the CJC1808 device receives the timing for data transfer from an external controller.

MD1 (PIN 11)	MD0 (PIN 10)	INTERFACE MODE
Low	Low	Slave mode (256 fS, 384 fS, 512 fS autodetection)
Low	High	Master mode (512 fs)
High	Low	Master mode (384 fs)
High	High	Master mode (256 fs)

Table 2. Interface Modes

7.3.5.2 Master Mode

In master mode, BCK and LRCK work as output pins, timing which from the clock circuit of the CJC1808 device controls these pins. The frequency of BCK is constant at 64 BCK/frame.

7.3.5.3 Slave Mode

In slave mode, BCK and LRCK work as input pins. The CJC1808 device accepts 64-BCK/frame or 48-BCK/frame format (only for a 384-fs system clock), not 32-BCK/frame format.

7.3.5.4 Data Format

NO.	FMT (Pin 12)	FORMAT
0	Low	I2S, 24-bit
1	High	Left-justified, 24-bit

Table 3. Data Format

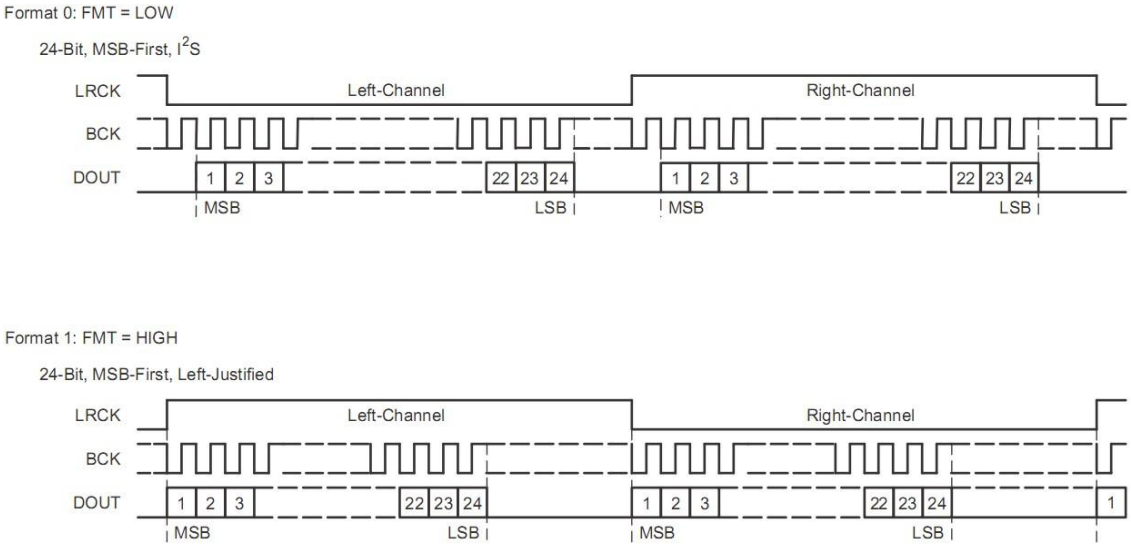


Figure 24. Audio Data Format (LRCK and BCK Work as Inputs in Slave Mode and as Outputs in Master Mode)

7.3.5.5 Interface Timing

Figure 4 and Figure 5 illustrate the interface timing in slave mode and master mode, respectively.

7.4 Device Functional Modes

7.4.1 Fade-In and Fade-Out Functions

The CJC1808 device has fade-in and fade-out functions on DOUT (pin 9) to avoid pop noise, and the functions come into operation in some cases as described in several following sections. Performance of the level changes from 0 dB to mute or mute to 0 dB employs calculated pseudo S-shaped characteristics with zero-cross detection. Because of the zero-cross detection, the time needed for the fade-in and fade-out depends on the analog input frequency (fin). It takes 48 / fin to complete the processing. If there is no zero-cross during 8192 / fs,a forced DOUT fade-in or fade-out occurs during 48 / fs (TIME OUT). Figure 25 illustrates the fade-in and fade-out operation processing.

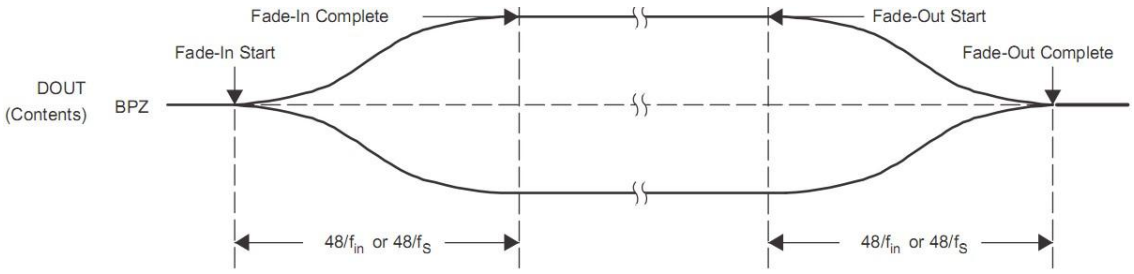


Figure 25. Fade-In and Fade-Out Operations

7.4.2 Clock-Halt Power-Down and Reset Function

The CJC1808 device has a power-down and reset function. Halting SCKI (pin 6) in both master and slave modes triggers this function. The function is available any time after power on. Reset and power down occur automatically 4 μs (minimum) after the halt of SCKI. During assertion of the clock-halt reset, the CJC1808 device stays in the reset and power-down mode, with DOUT (pin 9) forced to zero. Release the reset and power-down mode requires the supply of SCKI. The digital output is valid after release of the reset state and elapse of the time of 1024 SCKI + 8960 / fs. Performing the fade-in operation takes additional time of 48 / fin or 48 / fs to attain the level corresponding to the analog input signal. Figure 3 illustrates the clock-halt reset timing.

To avoid ADC performance degradation, BCK (pin 8) and LRCK (pin 7) must synchronize with SCKI within 4480/ fs after the resumption of SCKI. If it takes more than 4480 / fs for BCK and LRCK to synchronize with SCKI,mask SCKI until it again achieves synchronization, taking care of glitch and jitter. See the typical circuit connection diagram, Figure 26.

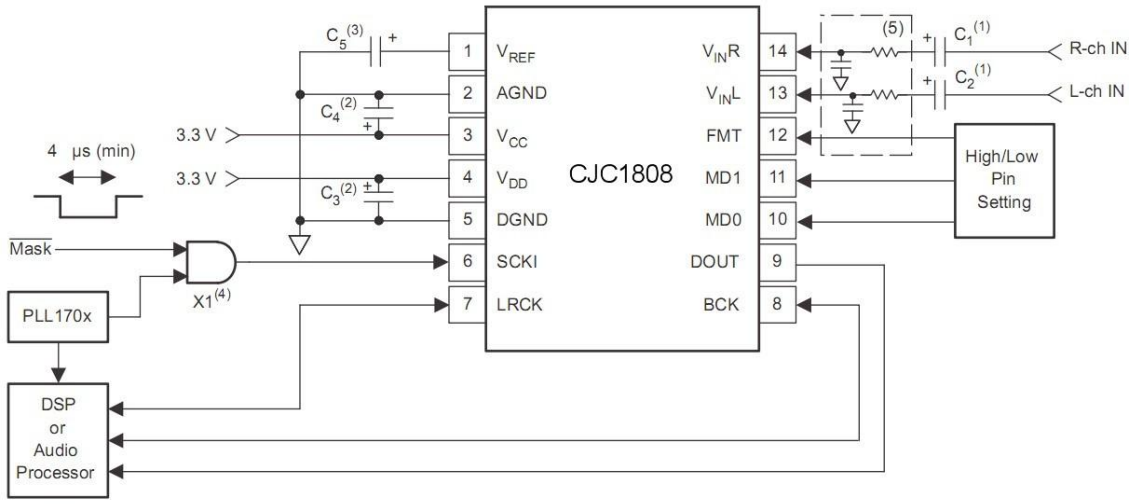
To avoid ADC performance degradation, assertion of the clock-halt reset is necessary when changing system clock SCKI or the audio interface clocks BCK and LRCK (sampling rate fs) on the fly.

8. Application and Implementation

8.1 Application Information

The CJC1808 device is suitable for wide variety of cost-sensitive consumer applications requiring good performance and operation with a 3.3-V analog supply and 3.3-V digital supply.

8.2 Typical Application



(1) C1, C2: A 1-µF electrolytic capacitor gives 2.7 Hz (τ = 1 µF × 60 kΩ) cutoff frequency for the input HPF in normal operation and requires a power-on settling time with a 60-ms time constant in the power-on initialization period.

(2) C3, C4: Bypass capacitors, 0.1-µF ceramic and 10-µF electrolytic, depending on layout and power supply

(3) C5: Recommended capacitors are 0.1-µF ceramic and 10-µF electrolytic.

(4) X1: X1 masks the system clock input when using the clock-halt reset function with external control.

(5) Optional external antialiasing filter could be required, depending on the application.

Figure 26. Typical Circuit Connection Diagram

8.2.1 Design Requirements

CJC1808 For this design example, use the parameters listed in Table 4 as the input parameters.

DESIGN PARAMETER	EXAMPLE VALUE
Analog input voltage range	0 Vp-p to 1.8 Vp-p
Output	PCM audio data
System clock input frequency	2.048 MHz to 49.152 MHz
Output sampling frequency	8 kHz to 96 kHz
Power supply	3.3 V

Table 4. Design Parameters

9. Power Supply Recommendations

The CJC1808 device requires a 3.3-V nominal supply and a 3.3-V nominal supply. The 3.3-V supply is for the analog circuitry powered by the VCC pin. The 3.3-V supply is for the digital circuitry powered by the VDD pin. The decoupling capacitors for the power supplies should be placed close to the device terminals.

A VCC that varies from the nominal 3.3 V affects the reference voltage for the input. This has a slight impact on the data conversion of the device.

10. Layout

10.1 Layout Guidelines

10.1.1 VCC, VDD Pins

Bypass the digital and analog power supply lines to the CJC1808 device to the corresponding ground pins with both 0.1-μF ceramic and 10-μF electrolytic capacitors as close to the pins as possible to maximize the dynamic performance of the ADC.

10.1.2 AGND, DGND Pins

To maximize the dynamic performance of the CJC1808 device, there are no internal connections to the analog and digital grounds. These grounds should have low impedance to avoid digital noise feedback into the analog ground. They should be connected directly to each other under the CJC1808 device package to reduce potential noise problems.

10.1.3 VINL, VINR Pins

VINL and VINR are single-ended inputs. These inputs have integrated antialias low-pass filters to remove the high-frequency noise outside the audio band. If the performance of these filters is not adequate for an application, the application requires appropriate external antialiasing filters. An appropriate choice would typically be a passive RC filter in the range of 100 Ω and 0.01 μF to 1 kΩ and 1000pF.

10.1.4 VREF Pin

To ensure low source impedance of the ADC references, the recommended capacitors between VREF and AGND are 0.1-μF ceramic and 10-μF electrolytic. These capacitors should be located as close as possible to the VREF pin to reduce dynamic errors on the ADC references.

10.1.5 DOUT Pin

The DOUT pin has a large load-drive capability, but if the DOUT line is long, a recommended practice is to locate a buffer near the CJC1808 device and minimize load capacitance to minimize the digital-analog crosstalk and maximize the dynamic performance of the ADC.

10.1.6 System Clock

The quality of the system clock can influence dynamic performance, as the CJC1808 device operates based on a system clock. Therefore, it may be necessary to consider the system clock duty, jitter, and the time difference between system clock transition and BCK or LRCK transition in slave mode.

10.2 Layout Example

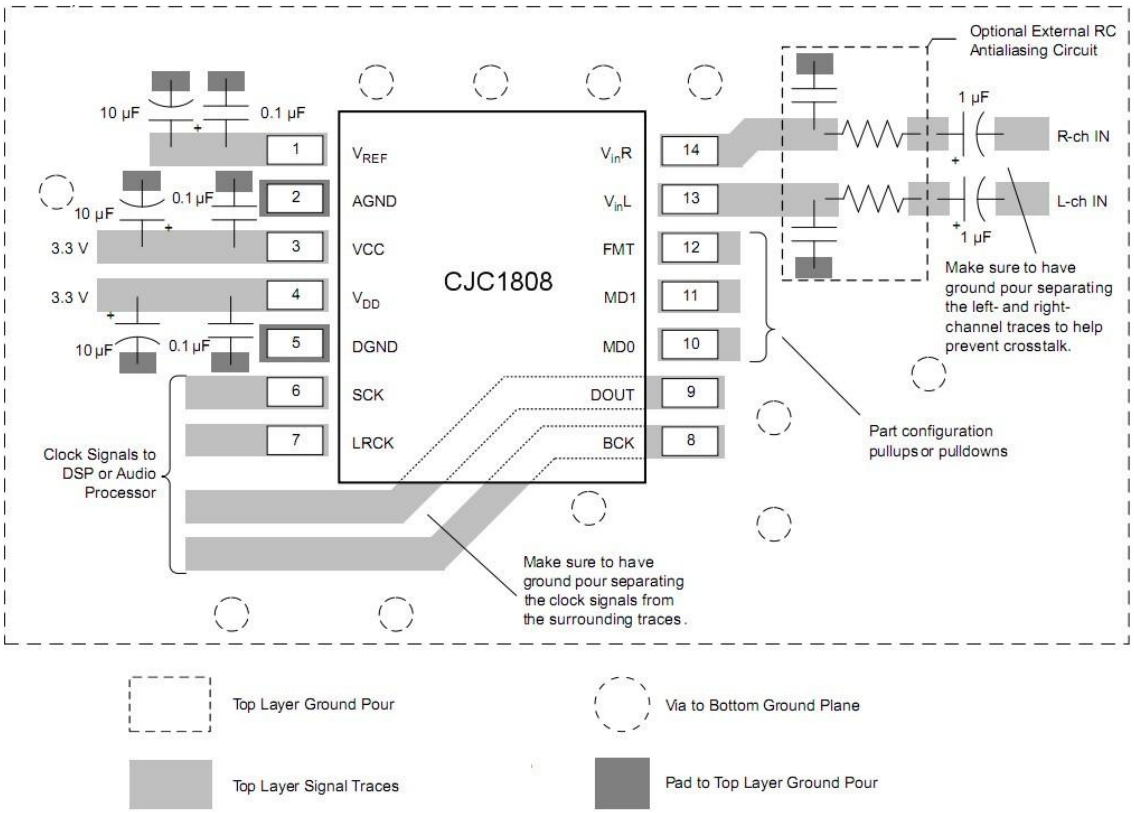
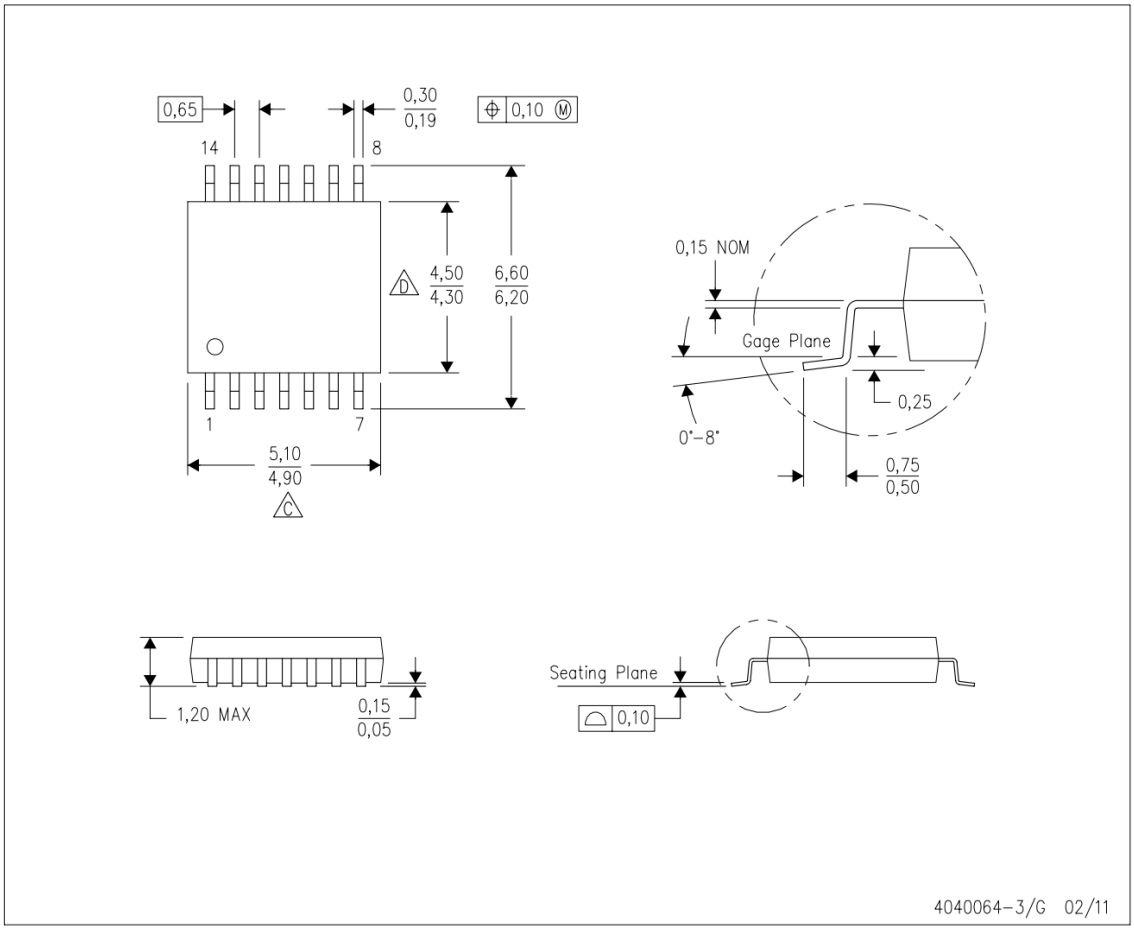


Figure 27. CJC1808 Layout Example

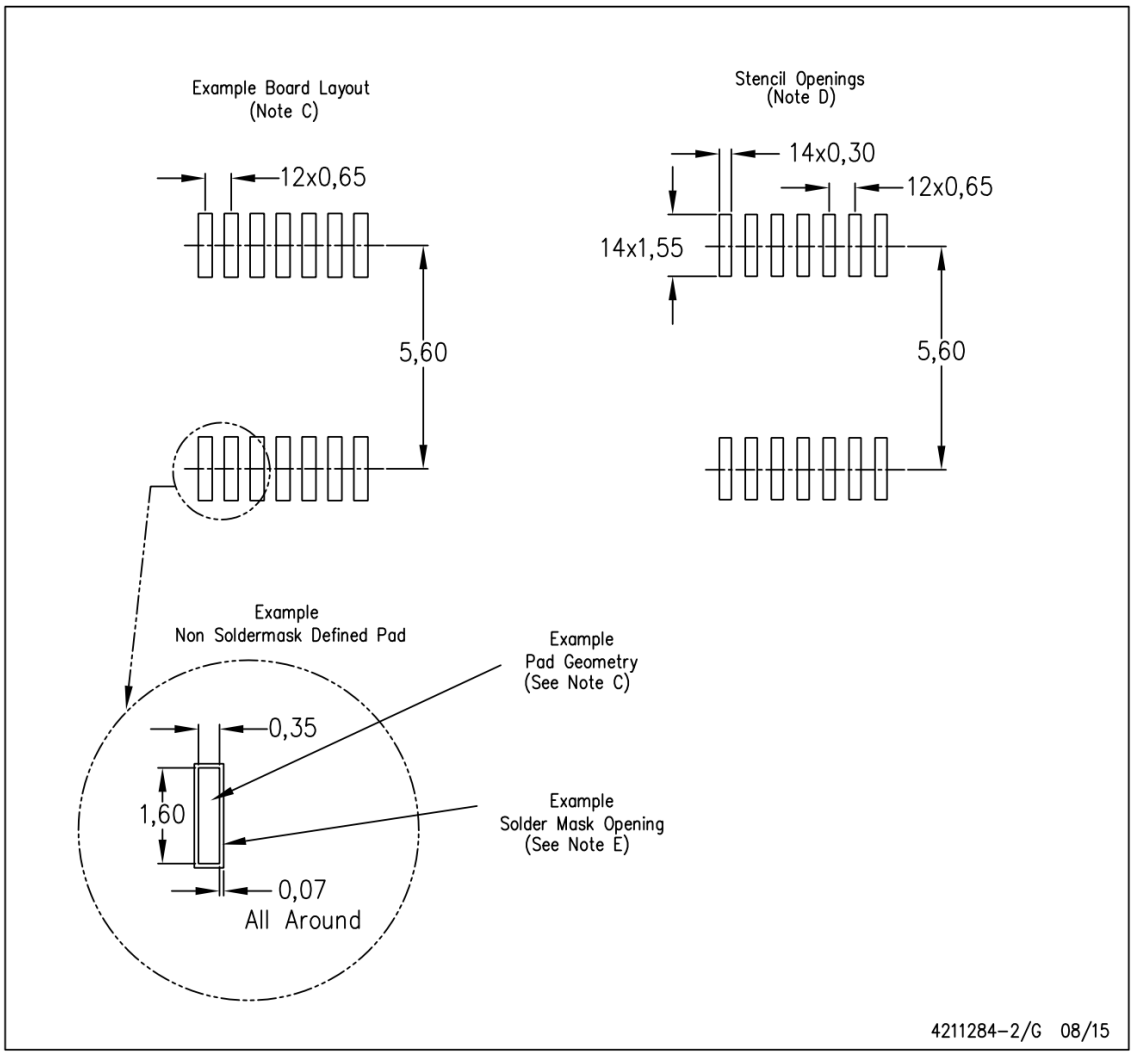
11. PACKAGE DIMENSIONS

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.