APT32F1023 Data sheet V1.5

Related documents

APT32F102X Series User Manual

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Historical version description

Release	Modified date	Modification summary
V0.0	2020-11-24	First edition
V1.0	2020-12-01	Revise obvious errors in the first version
V1.1	2020-12-07	No errors found in the revised V1.0 part
V1.2	2021-01-08	Update logo
V1.3	2021-02-01	Correct TTL, SWD, FIN, Flash related content
V1.4	2021-03-30	Correct LVD errors & English version established
V1.5	2021-05-31	Correct Translation

1 Overview

1.1 APT32F1023 Introduction

APT32F1023 is a 32-bit, high-performance, low-cost microcontroller developed by APT Microelectronics based on the T-HEAD Semiconductor CPU core. The applications of APT32F1023 single-chip microcomputer are industrial control, touch home appliances, consumer electronic equipment, wearable devices and other applications.

- C-Sky 32-bit CPU core (0.7DMIPS), supports single-cycle multiplication and SWD debugging
- Independent hardware divider
- On-chip 64K (32Kbytes optional) program flash memory, independent 2Kbytes data flash memory

Contains 4Kbytes SRAM, which can be used for stack, data storage, code storage

- Working temperature: 40 to 85 C
- Operating voltage range: 1.8 to 5.5V
- Maximum operating frequency: 48MHz
- Interrupt Controller: Supports dynamically configured nestable interrupts (NVIC)
- Enhanced clock and power controller (SYSCON)
- Independent Watchdog Timer (IWDT)
- 1x16-bit enhanced timer/counter (EPT), each TIMER supports 4 PWM output functions, and supports complementary dead zone mode
- 1x 16-bit general-purpose timer/counter, supporting 2 PWM output functions (GPT)
- 1x 16-bit counter (COUNTERA), support automatic reload function and single or cycle counting function (carrier generator)
- 1x 16-bit basic timer TIMER (Basic Timer)
- 1x 16-bit low-power TIMER (LPT)
- 1x 16-bit RTC
- 1x 8-bit WWDT
- Serial communication interface: 1x I2C, 3x UART, 1/0 x SPI, 1 x SIO
- Up to 16 channels of 12-bit ADC, supporting internal/external VREF input
- Support 96bit UID function
- Supports up to 22 GPIOs, all GPIOs can be configured as external interrupts
- Support three working modes: RUN, SLEEP, and DEEP-SLEEP mode
- Up to 17 touch button controllers
- 4 high-current drive pins (each pin supports a maximum current of 120mA)

1.2 Main features

1.2.1 Processor（CPU）

- 32-bit RISC CPU core, 16-bit instruction length
- 16 32-bit general registers
- Efficient 2-level execution pipeline
- Single-cycle 32-bit x 32-bit hardware shaped multiplication array (the result only supports 32-bit)
- SWD (Serial Wire Debug) debug interface

1.2.2 Hardware divider（HWDIV）

- Signed or unsigned 32-bit integer division operation
- Support 32-bit dividend and 32-bit divisor, output 32-bit quotient and remainder
- 5 HCLK cycles operation time
- Supports divide-by-zero overflow error interrup

1.2.3 Memory

- 64Kbytes (32Kbytes optional) internal program flash memory, support ISP protection, configurable protection area size, support hardware CRC check
- 2Kbytes of independent data flash memory, data flash memory programming does not affect program operation
- User Option configuration
    - External reset pin enable configuration
    - Watchdog default enabled state configuration
    - Code security configuration
- Dedicated programming interface, supporting rapid mass production programming (need to cooperate with a dedicated programming device)
- Up to 4Kbytes of internal SRAM, support hardware CRC check
- Little-endian storage method

1.2.4 Nestable interrupt controller（NVIC）

- Up to 32 interrupt sources, support interrupt vector table redirection
- 32 programmable priority levels, each interrupt has an independent priority level
- Each interrupt has independent enable or disable control
- Each interrupt source has a fixed vector address
- Support trap function
- Support software reset
- Global interrupt enable control

- Enable/disable wake-up events can be individually configured (can be configured to not enter interrupts after wake-up)

1.2.5 System Controller(SYSCON)

- External crystal oscillator 400KHz to 24MHz (EMCLK: External Main Clock, external main clock), support independent 32.768K configuration items
- Internal main oscillator 131.072KHz / 2.097MHz / 4.194MHz / 5.556MHz (default) four option selections (1% deviation@typical value, IMCLK: Internal Main Clock, internal main clock)
- Internal high-speed oscillator 24MHz/48MHz (1% deviation@typical value, HFCLK: High Frequency Clock, internal high-speed clock)
- Internal auxiliary oscillator 27KHz (5% deviation@typical value, ISCLK: Internal Sub Clock, internal auxiliary clock)
- All internal oscillators support software fine-tuning
- Support low power consumption mode (SLEEP/DEEP-SLEEP)
- Support programmable power optimization in low power mode
- Programmable clock divider
- External crystal oscillator failure monitoring (when the external crystal oscillator fails, it supports automatic switching to the internal main oscillator)
- External crystal jitter filter processing
- External interrupt input digital filter control, support asynchronous counting triggered by interrupt
- FLASH and SRAM check error management, configurable retry or system reset
- Reset source detection and management (RSTID)

1.2.6 Independent watchdog timer（IWDT）

- Configurable reset time: 8 seconds by default
- Configurable alarm interrupt before reset
- Programmable 18-bit down counter (27KHz clock) independently working under the internal auxiliary crystal oscillator

1.2.7 16-bit enhanced timer/counter（EPT）

- Three counting modes: increment, decrement, increment and decrement
- Each TIMER has 4 independent PWM outputs and supports 4 comparison values
- Support complementary output, dead zone control, chopping output, emergency mode output
- Support emergency mode output: soft lock and hard lock mode
    - External input EPIx
    - System error, LVD interrupt triggered
- Support special register protection
- Support single trigger mode and external pulse counting mode

- 4 digital comparators can trigger a variety of synchronization and waveform output
- Can work in capture mode, support up to 4 comparison value capture
- Support ETCB event linkage
- PCLK working clock

1.2.8 16 Bit general-purpose timer/counter（GPT）

- Three counting modes: increment, decrement, increment and decrement
- Each TIMER supports two output channels, and each channel can be configured as PWM waveform output control
- Support capture mode, up to 4 capture values
- Support ETCB event linkage
- PCLK working clock

1.2.9 Counter A (CNTA)

- 1 16-bit counter, support automatic reload function and single or cycle counting function
- Software/hardware selectable carrier frequency output enable/disable control
- Within a periodic waveform, the output high/low pulse width is configurable
- Configurable output polarity
- Can be used to drive speakers or remote IR data transmission

1.2.10 Basic timer (BT)

- 1 16-bit up counter, supporting automatic reload function
- A comparison value register, supporting PWM waveform output
- Support single trigger mode
- Support comparison value Match interrupt, periodic interrupt and overflow interrupt
- Support ETCB event linkage
- PCLK working clock

1.2.11 Core Timer (CORET)

- 1 24-bit down counter, supporting automatic reload function
- Counting clock source is optional (CPU clock or system clock divided by 8)
- Support periodic interrupt and overflow interrupt

1.2.12 Low Power Timer (LPT)

- 16-bit up counter, support auto reload function
- A 16-bit comparison value register, supporting PWM output
- 3-bit prescaler selection, support 1, 2, 4, 8, 16, 32, 64, 128 frequency division
- Support multiple counting clock sources: ISCLK, IMCLK, EMCLK, PCLK or external CLK

- Support Toggle or PWM output function
- Support single trigger mode
- Support periodic interrupt and MATCH interrupt
- Support ETCB event linkage

1.2.13 Real Time Counter（RTC）

- Only POR reset is valid, support write protection
- Timing function: support hour (12 or 24 hour format), minutes, seconds and sub-seconds, BCD format
- Calendar function: support year, month, day and week, BCD format; automatic leap year recognition
- Support optional clock sources: external crystal oscillator EMCLK (support 32.768KHz), internal main oscillator IMCLK and internal secondary oscillator ISCLK.
- Support 2 programmable alarm clocks
- Support periodic timer interrupt
- Digital calibration function
- Support ETCB event linkage
- Programmable frequency output (output through CLO)

1.2.14 Window Watchdog（WWDT）

- Work based on PCLK
- Support alarm interrupt before reset
- Reset operation can be triggered by software
- Counter refresh window limit function

1.2.15 Universal Asynchronous Receiver Transmitter（UART）

- 2 channels
- 8-bit data length, support parity bit (parity check, 0/1 check)
- Separate 8x8 bit transceiver FIFO
- Programmable fractional baud rate generator

1.2.16 Synchronous serial bus（I2C）

- 1 channel
- Support multi-master I2C bus, support master or slave working mode.
- Standard mode 100Kbit/s, high-speed mode up to 400Kbit/s, ultra-high-speed mode up to 1Mbit/s
- Compatible with serial 8-bit data transmission and two-way data transmission
- 7-bit or 10-bit addressing
- Programmable SDA hold time
- Automatic bus recovery function

- Separate 8x8 bit transceiver FIFO

1.2.17 Synchronous serial bus（SPI）

- 1/0 channel
- Programmable data frame length: 4 to 16 bits
- Support host and slave mode
- Programmable clock prescaler
- Support single-line transceiver mode
- Separate 8x16-bit transceiver FIFO

1.2.18 Serial input and output interface（SIO）

- 1 channel, single-wire communication interface, two-way data transmission
- Custom communication protocol and waveform output
- In output mode, it supports continuous output of 16 Patterns
- In the receiving mode, it supports continuous 32bit or pattern reception, hardware sampling and automatic extraction, and input filtering

1.2.19 12bit AD Converter

- Up to 16 analog input channels for selection, the reference voltage supports VDD, external pins, INTVREF or FVR
- ADC input supports external ADCIN, GND, 1/4VDD and internal high-precision voltage reference source (INTVREF)
- Support the fastest 1MSPS conversion speed
- Configurable sample and hold time
- Support continuous conversion mode and hardware automatic comparison of conversion results
- Support multi-sequence conversion mode, up to 16 conversion sequences, flexible configuration of conversion channels, conversion order, conversion times, sequence priority
- Support ETCB event linkage

1.2.20 Internal Voltage Reference（INTVREF）

- As ADC sampling channel calibration input
- As VREF input of ADC (ADC must work in low speed state)
- Reference voltage: 1.0V

1.2.21 Fixed Voltage Reference（FVR）

- As VREF input of ADC
- Reference voltage: 2.048V/4.096V

1.2.22 Touch Key Sensor（TKEY）

- Self-capacitance detection analog front end based on charge transfer principle

- Support scanning frequency spread spectrum, randomized configuration, improve anti-jamming performance
- Support 17 scanning channels
- Support sequence scanning, the sequence supports up to 18 configuration units
- Independent programmable sensitivity adjustment for each channel
- Multiple scan trigger modes
- Support hardware automatic key detection and system wake-up

1.2.23 Check the controller（CRC）

- Support writing operations based on Byte, Half-word, Word
- The selectable CRC polynomials include:
  - CRC-CCITT：$X^{16} + X^{12} + X^5 + 1$
  - CRC-16：$X^{16} + X^{15} + X^2 + 1$
  - CRC-32：$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^3 + X^2 + X + 1$
- Programmable seed value
- Input data and output data (CRC checksum) can be converted into complementary code operation
- Programmable bit reversal setting (LSB first or MSB first)

1.2.24 Event Trigger Cross Bar（ETCB）

- Supports configurable interconnect triggering between on-chip modules
- Support up to 8 trigger channels
- Each channel supports 64 Source input options
- Each channel supports 64 Target output options
- Each channel supports software trigger

1.2.25 General IO (GPIO)

- 24 pins: 22 GPIO
- 20 pins: 18 GPIO
- 16 pins: 14 GPIO
- Push-pull output and open-drain output are configurable, pull-up and pull-down resistors are configurable
- The output can be independently configured with drive capacity and slope
- Support output status monitoring
- The communication port supports TTL level input buffer configuration (TTL1/TTL2)
- All pins support external interrupt function

1.2.26 Two low-power modes

- SLEEP: Turn off the selected system clock and CPU clock
- DEEP-SLEEP: Turn off all system clocks and CPU clocks

- Configurable DEEP-SLEEP wake-up source: external interrupt, iWDT interrupt, LPT interrupt, LVD interrupt, RTC interrupt or touch button interrupt

1.2.27 Power On Reset（POR）

1.2.28 Low Voltage Detector（LVD）

- Configurable low voltage reset function, optional 8 voltage values (1.9V/2.2V/2.5V/2.8V/3.1/3.4/3.7/4.0).
- Configurable low voltage interrupt, select 7 detection voltage values (2.1V/2.4V/2.7V/3.0V/3.3/3.6/3.9)

1.2.29 Operating voltage range

- 1.8V to 5.5V

1.2.30 Operating frequency range

- External main crystal oscillator: 32KHz ~ 24 MHz
- Internal oscillator: IMOSC: 5.556 MHz (max) / HFOSC: 48 MHz (max)
- Internal auxiliary vibration: 27KHz

1.2.31 Operating temperature range

- – 40 to 85°C

1.2.32 Package

- SSOP24
- SOP24
- SOP20
- QFN20
- SOP16

1.3 Block diagram

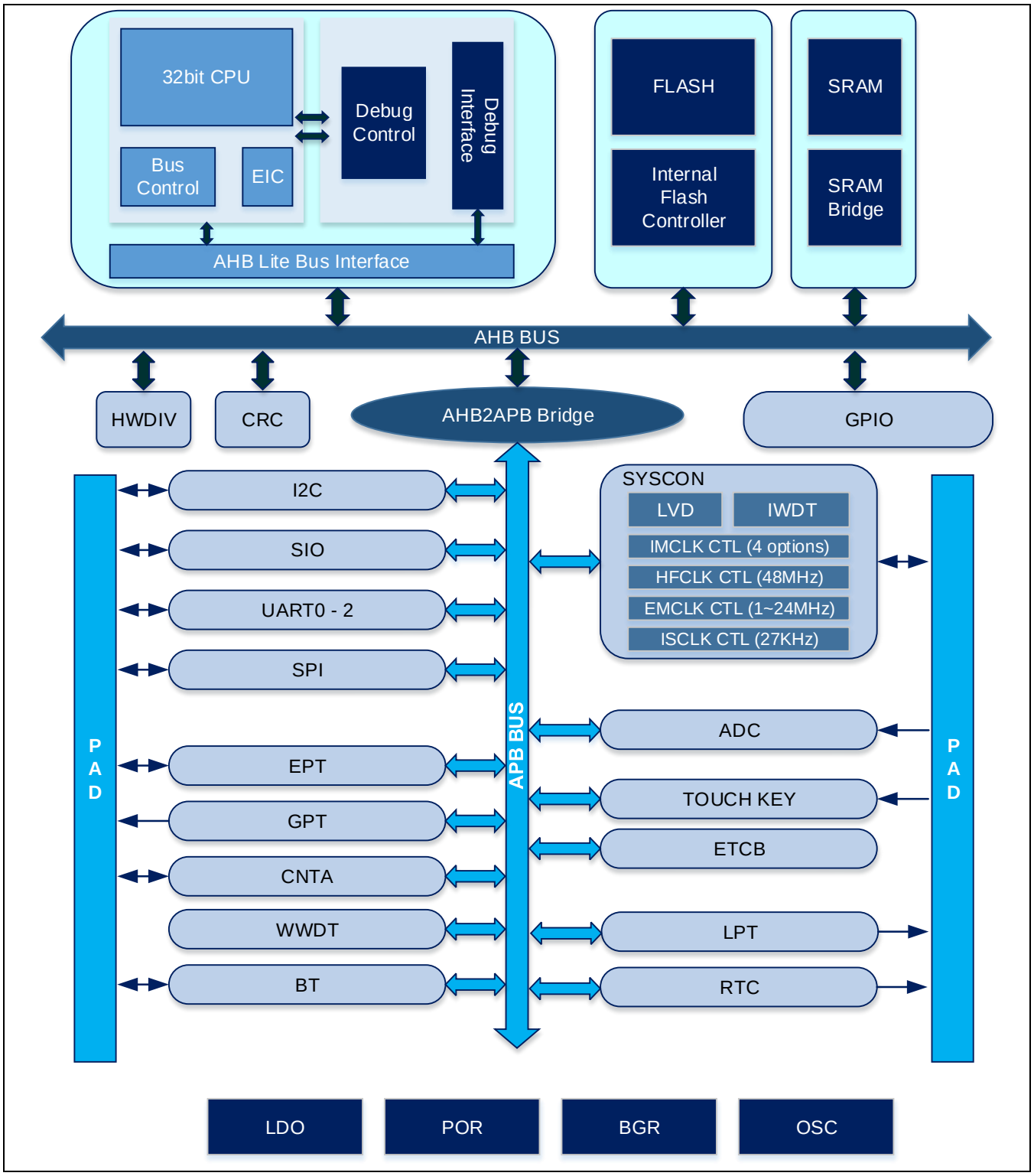


Figure 1-1 APT32F1023 Block diagram

2 Pin configuration

2.1 Summary

This chapter describes the pin function information of the APT32F1023 product.

contain:

- Pin map
- Pin allocation table
- Remap pin
- Pin description
- Pad circuit type

2.2 Pin definition diagram

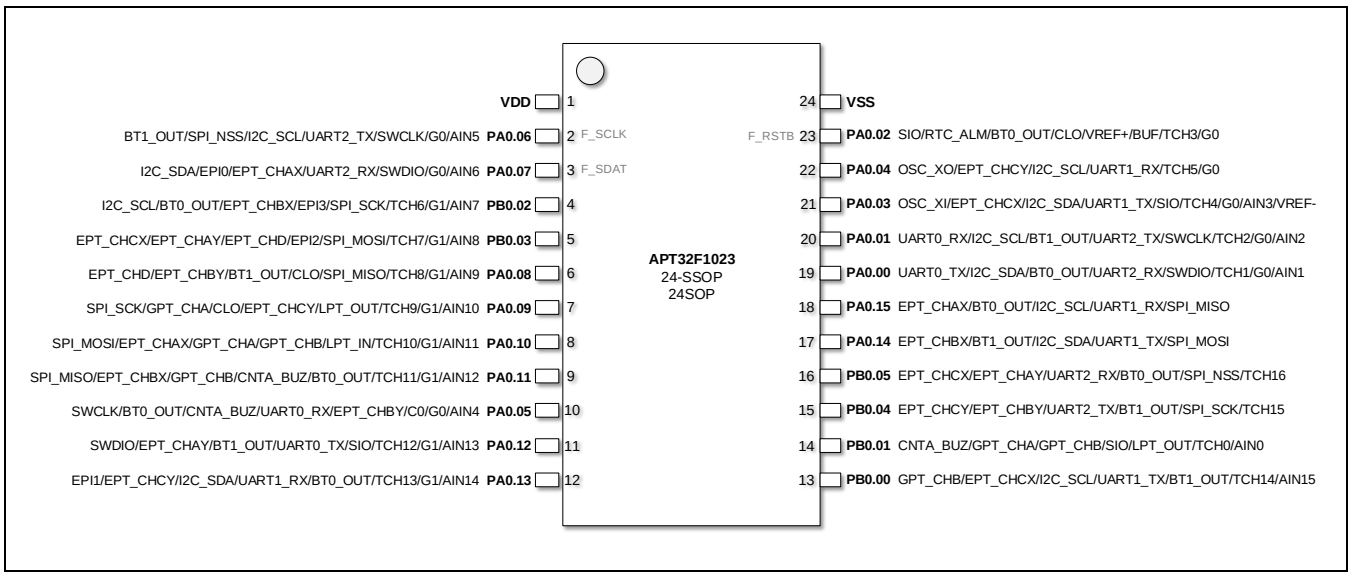


Figure 2-1 Pin definition diagram (24PIN)

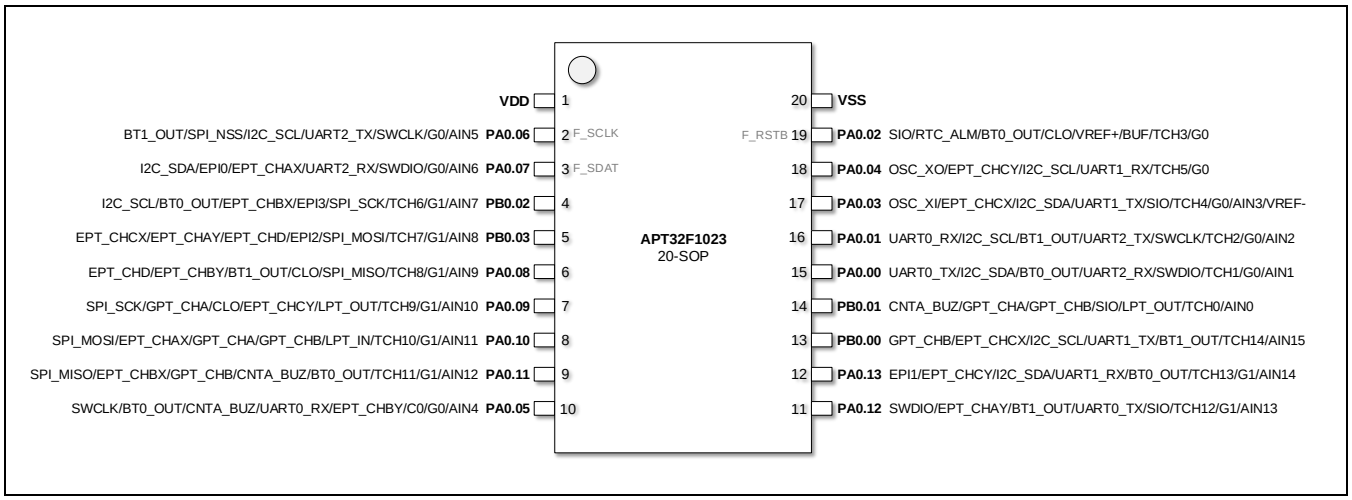


Figure 2-2 Pin definition diagram (20SOP)

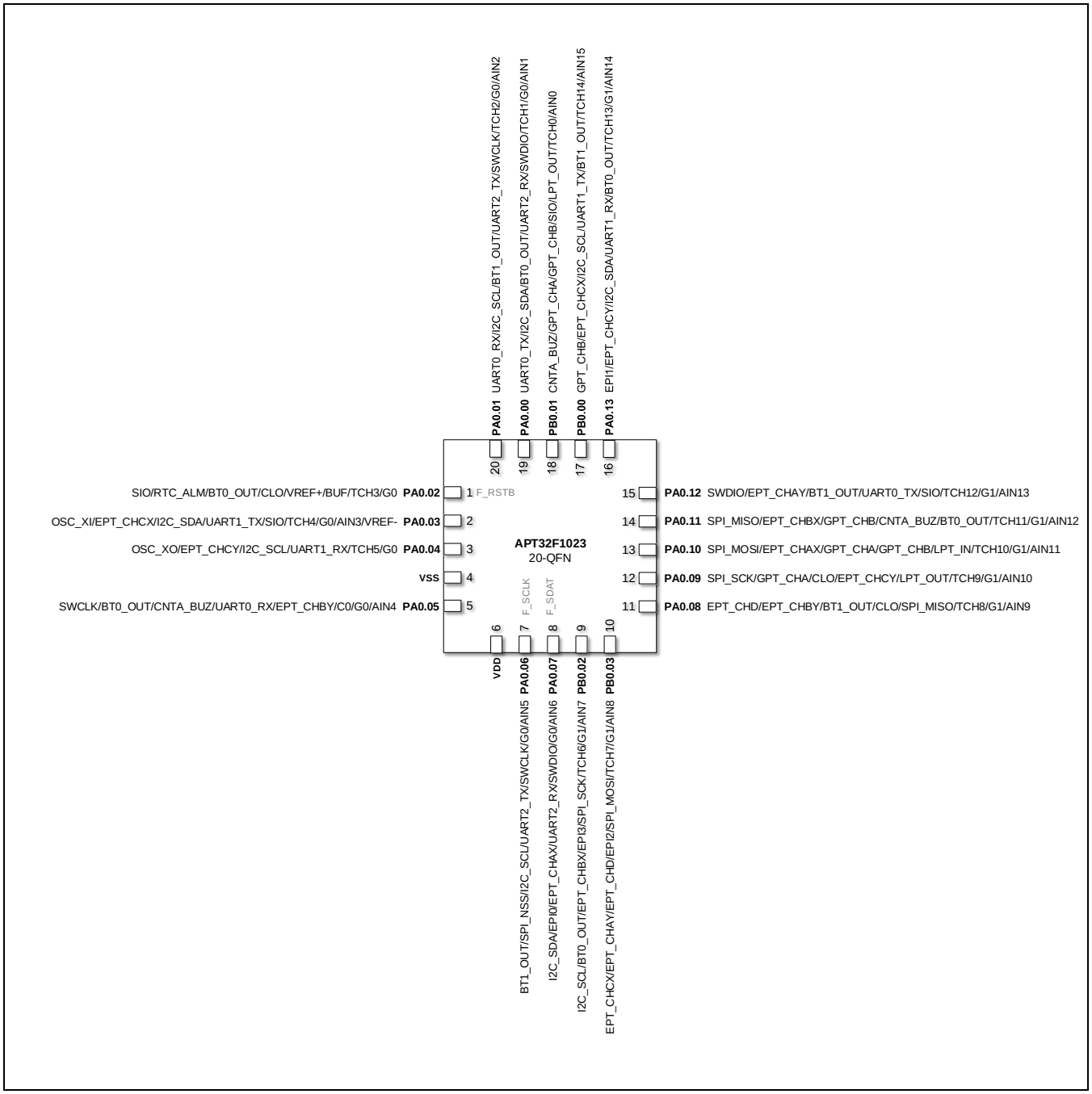


Figure 2-2 Pin definition diagram (20QFN)

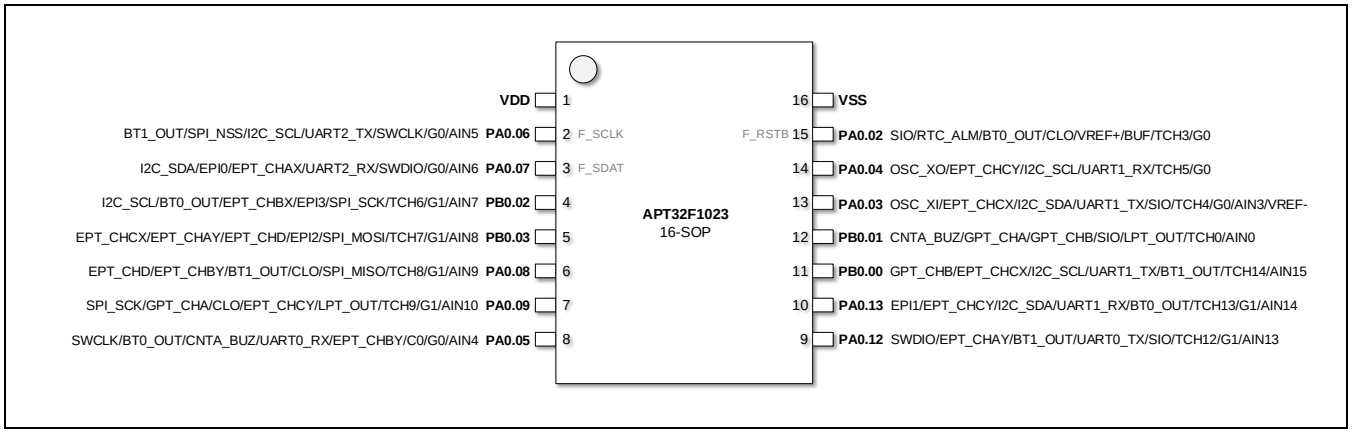


Figure 2-3 Pin definition diagram (16PIN)

2.3 Pin function allocation

Table 2-1 describes the detailed allocation of pin functions.

- *UP*: pull-up enable; *DN*: pull-down enable; *IO*: bidirectional; *I*: input; *O*: output; *P*: power; *G*: ground; *Z*: high impedance

Table 2-1 Pin function allocation

Package					Pin Name										Default	TTL Mode	Reset Status
24SSOP	24SOP	20SOP	20QFN	16SOP	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	EXI			
1	1	1	6	1	VDD	-	-	-	-	-	-	-	-	VDD	PWR	-	P
2	2	2	7	2	PA0.6	BT1_OUT	SPI_NSS	I2C_SCL	UART2_TX	**SWCLK**	-	G0	AIN5	EXI6	SWCLK	B	I
3	3	3	8	3	PA0.7	I2C_SDA	EPI0	EPT_CHAX	UART2_RX	**SWDIO**	-	G0	AIN6	EXI7	SWDIO	B	I
4	4	4	9	4	PB0.2(HS)	I2C_SCL	BT0_OUT	EPT_CHBX	EPI3	SPI_SCK	TCH6	G1	AIN7	EXI2	IO	S	Z
5	5	5	10	5	PB0.3(HS)	EPT_CHCX	EPT_CHAY	EPT_CHD	EPI2	SPI_MOSI	TCH7	G1	AIN8	EXI3	IO	-	Z
6	6	6	11	6	PA0.8(HS)	EPT_CHD	EPT_CHBY	BT1_OUT	CLO	SPI_MISO	TCH8	G1	AIN9	EXI8	IO	-	Z
7	7	7	12	7	PA0.9(HS)	SPI_SCK	GPT_CHA	CLO	EPT_CHCY	LPT_OUT	TCH9	G1	AIN10	EXI9	IO	-	Z
8	8	8	13	-	PA0.10	SPI_MOSI	EPT_CHAX	GPT_CHA	GPT_CHB	LPT_IN	TCH10	G1	AIN11	EXI10	IO	-	Z
9	9	9	14	-	PA0.11	SPI_MISO	EPT_CHBX	GPT_CHB	CNTA_BUZ	BT0_OUT	TCH11	G1	AIN12	EXI11	IO	-	Z
10	10	10	5	8	PA0.5	**SWCLK**	BT0_OUT	CNTA_BUZ	UART0_RX	EPT_CHBY	C0	G0	AIN4	EXI5	IO	-	Z
11	11	11	15	9	PA0.12	**SWDIO**	EPT_CHAY	BT1_OUT	UART0_TX	SIO	TCH12	G1	AIN13	EXI12	IO	-	Z
12	12	12	16	10	PA0.13	EPI1	EPT_CHCY	I2C_SDA	UART1_RX	BT0_OUT	TCH13	G1	AIN14	EXI13	IO	B	Z
13	13	13	17	11	PB0.0	GPT_CHB	EPT_CHCX	I2C_SCL	UART1_TX	BT1_OUT	TCH14	-	AIN15	EXI0	IO	B	Z
14	14	14	18	12	PB0.1	CNTA_BUZ	GPT_CHA	GPT_CHB	SIO	LPT_OUT	TCH0	-	AIN0	EXI1	IO	-	Z
15	15	-	-	-	PB0.4	EPT_CHCY	EPT_CHBY	UART2_TX	BT1_OUT	SPI_SCK	TCH15	-	-	EXI4	IO	-	Z
16	16	-	-	-	PB0.5	EPT_CHCX	EPT_CHAY	UART2_RX	BT0_OUT	SPI_NSS	TCH16	-	-	EXI5	IO	-	Z
17	17	-	-	-	PA0.14	EPT_CHBX	BT1_OUT	I2C_SDA	UART1_TX	SPI_MOSI	-	-	-	EXI14	IO	B	Z
18	18	-	-	-	PA0.15	EPT_CHAX	BT0_OUT	I2C_SCL	UART1_RX	SPI_MISO	-	-	-	EXI15	IO	B	Z
19	19	15	19	-	PA0.0	UART0_TX	I2C_SDA	BT0_OUT	UART2_RX	**SWDIO**	TCH1	G0	AIN1	EXI0	IO	S	Z
20	20	16	20	-	PA0.1	UART0_RX	I2C_SCL	BT1_OUT	UART2_TX	**SWCLK**	TCH2	G0	AIN2	EXI1	IO	S	Z
21	21	17	2	13	PA0.3	OSC_XI	EPT_CHCX	I2C_SDA	UART1_TX	SIO	TCH4	G0	AIN3/VREF-	EXI3	IO	S	Z
22	22	18	3	14	PA0.4	OSC_XO	EPT_CHCY	I2C_SCL	UART1_RX	-	TCH5	G0	-	EXI4	IO	S	Z
23	23	19	1	15	PA0.2	SIO	RTC_ALM	BT0_OUT	CLO	VREF+/INTV	TCH3	G0	-	EXI2	IO	-	Z
24	24	20	4	16	**VSS**	-	-	-	-	-	-	-	-	VSS	GND	-	G

Note：

1) The external reset function is multiplexed with the PA0.2 pin, you can use the User Option function to select the configuration

2) F_SCLK, F_SDAT, F_RSTB are the interface signals of the external flash memory burning tool

3) As long as each IO pin is configured as a digital IO function, the EXI function can be used to trigger an interrupt

4) There are a total of three groups of optional SWD interfaces. The SWD pins can be remapped using the chip burner. The default interfaces are PA0.6 and PA0.7. During the debugging process, do not modify the AF function of SWD to other AF functions, otherwise the debugging connection will be lost and the debugger can no longer be connected.

5) In the TTL Mode column, S indicates that the pin only supports TTL1 level, B indicates that it supports both TTL1 and TTL2 levels. Refer to the GPIO chapter for the configuration method

6) The IO marked with the (HS) symbol is a high current drive port (High Sink Current IO), which supports a sink current of 120mA. Refer to the GPIO chapter for configuration methods

7) AF7 G0/G1 is the IO redefinition function, you can freely define the IO AF function, the specific configuration method refers to the IO redefinition in the SYSCON chapter

2.4 Function pin mapping

The related functions of each peripheral can be selected through the AF function setting of GPIO. Some multiplexed functions have remapped pins, which is convenient for users to use various functions in various applications.

Table 2-2 Overview of peripheral function mapping

functional module	Function Pins	Pin Assignment
EPT	EPT_CHAX(O)	PA0.7/PA0.10/PA0.15
	EPT_CHAY(O)	PB0.3/PB0.5/PA0.12
	EPT_CHBX(O)	PB0.2/PA0.11/PA0.14
	EPT_CHBY(O)	PA0.5/PA0.8/PB0.4
	EPT_CHCX(O)	PA0.3/PB0.0/PB0.3/PB0.5
	EPT_CHCY(O)	PA0.4/PA0.9/PA0.13/PB0.4
	EPT_CHD(O)	PB0.3/PA0.8
	EPI0(I)	PA0.7
	EPI1(I)	PA0.13
	EPI2(I)	PB0.3
	EPI3(I)	PB0.2
GPT	GPT_CHA(O)	PB0.1/PA0.9/PA0.10
	GPT_CHB(O)	PA0.10/PA0.11/PB0.0/PB0.1
BT0	BT0_OUT	PA0.0/PA0.2/PA0.5/PB0.2/PB0.5/PA0.11/PA0.13/PA0.15
BT1	BT1_OUT	PA0.1/PA0.6/PA0.8/PA0.12/PA0.14/PB0.0/PB0.4
CNTA	CNTA_BUZ(O)	PB0.1/PA0.5/PA0.11
LPT	LPT_OUT(O)	PB0.1/PA0.9
	LPT_IN(I)	PA0.10
RTC	RTC_ALM(O)	PA0.2
I2C	I2C_SCL(B)	PB0.0/PB0.2/PA0.1/PA0.4/PA0.6/PA0.15
	I2C_SDA(B)	PA0.0/PA0.3/PA0.7/PA0.13/PA0.14
UART0	UART0_TX(O)	PA0.0/PA0.12
	UART0_RX(I)	PA0.1/PA0.5
UART1	UART1_TX(O)	PB0.0/PA0.3/PA0.14
	UART1_RX(I)	PA0.13/PA0.4/PA0.15
UART2	UART2_TX(O)	PA0.1/PA0.6/PB0.4
	UART2_RX(I)	PA0.0/PA0.7/PB0.5
SPI	SPI_SCK(B)	PB0.2/PB0.4/PA0.9
	SPI_MOSI(B)	PB0.3/PA0.10/PA0.14

	SPI_MISO(B)	PA0.8/PA0.11/PA0.15
	SPI_NSS(O)	PA0.6/PB0.5
SIO	SIO(B)	PA0.2/PA0.3/PA0.12/PB0.1
SYSTEM	CLO(O)	PA0.2/PA0.8/PA0.9
	SWCLK(I)	PA0.5/PA0.6/PA0.1
	SWDIO(B)	PA0.12/PA0.7/PA0.0

Note：

1) For the output function, if multiple pins are configured to the same function, then all these pins will output the same signal.

2) For input function, if multiple pins are configured to the same function, the pin with the smaller AF number has higher priority. For example, when both PA0.5 and PA0.1 are configured as RX, only PA0.1 (AF1) is RX, and the RX configuration of PA0.5 (AF4) is invalid.

2.5 Pin function description

This paragraph describes the functions of the following pins:

- Power pin
- System function pins
- Common module function pins
- Debug interface pins
- Flash burning tool pins

Note：

1) D: digital; A: analog
2) I/O: bidirectional; I: input; O: output
3) P: power supply; G: ground
4) Z: High resistance

2.5.1 Power Pin

Table 2-3 Power pin description

Module	Pin Name	I/O	Pin Description	D/A
Power	VDD	-	Chip power	-
	VSS	-	Chip ground	-

2.5.2 System function pins

Table 2-4 System function pin description

Module	Pin Name	I/O	Pin Description	D/A
System	RSTB	I	Hardware reset input, when PA0.2 selects RESETB, there is a pull-up resistor inside	D
	XIN	I	External main crystal input	A
	XOUT	O	External main crystal output	A
	CLO	O	Internal system clock output	D

2.5.3 Common module function pins

Table 2-5 Common module function pin description

Module	Pin Name	I/O	Pin Description	D/A
GPIO	PA0.x	I/O	General IO A	D
	PB0.x	I/O	General IO B	D
EPT	EPT_CHAX	O	X output of channel A of EPT	D
	EPT_CHAY	O	Y output of channel A of EPT	D
	EPT_CHBX	O	X output of channel B of EPT	D
	EPT_CHBY	O	Y output of channel B of EPT	D
	EPT_CHCX	O	X output of channel C of EPT	D
	EPT_CHCY	O	Y output of channel C of EPT	D
	EPT_CHD	O	Channel D output of EPT	D
	EPIx	I	EPT emergency trigger signal	D
GPT	GPT_CHA	O	GPT channel A output	D
	GPT_CHB	O	GPT channel B output	D
BT	BTx_OUT	O	BT output	D
CNTA	CNTA_BUZ	O	Carrier frequency output of counter A	D
LPT	LPT_OUT	O	Waveform output of LPT	D
	LPT_IN	I	External input of LPT	D
RTC	RTC_ALM	O	RTC timing pulse output	D
I2C	I2C_SCL	I	I2C serial clock	D
	I2C_SDA	I/O	I2C serial data	D
UART	UARTx_RX	I	UART serial data reception	D
	UARTx_TX	O	UART serial data transmission	D
SPI	SPI_NSS	I/O	SPI chip select signal	D
	SPI_SCK	I/O	SPI synchronous clock signal	D
	SPI_MOSI	O	SPI data output port	D
	SPI_MISO	I	SPI data input port	D
SIO	SIO	I/O	SIO data input and output port	D
ADC	AINx	I	ADC analog input channel	A
	VREF+/-	I	ADC external reference voltage input signal	A
TOUCH	TCHx	I/O	Touch key scan channel	A
	C0	I/O	Touch button reference capacitor pin	A

2.5.4 Debug interface pins

Table 2-6 Debug interface pin description

Module	Pin Name	I/O	Pin Description	D/A
SWD	SWCLK	I	Serial clock, internal pull-up	D

	（PA0.5）			
	SWDIO （PA0.12）	I/O	Serial data input/output, internal pull-up	D

2.5.5 Pins of Flash Programming Tool

Table 2-7 Pin description of flash burning tool

Module	Pin Name	I/O	Pin Description	D/A
FLASH	F_SCL	I	Serial clock	D
	F_SDA	I/O	Serial data	D
	F_RSTB	I	Reset	D
	VDD	P	Power supply (It is recommended to connect a 0.1uF decoupling capacitor between VDD and VSS)	A
	VSS	G	Ground	A

3 Electrical characteristics

3.1 Limit parameters

If the device exceeds the following “limit parameters”, it may cause permanent damage. The device can only be guaranteed to work normally within the range of conditions specified in the manual. Working under the "limit parameter" condition will affect the reliability of the device.

Table 3-1 Limit parameters

Parameter	Symbol	Condition	Value	Unit
Operating Voltage	V_{DD}	–	–0.3 to 6.5	V
Input voltage	V_{IN}	–	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O	All ports	–0.3 to V_{DD} + 0.3	V
IO drive current	I_{SINK1}	Single ordinary IO injection	15	mA
		Single strong drive IO input	120	mA
	I_{SINK2}	Fill all IO	200	mA
	I_{SOURCE}	Single IO pull	15	mA
Working temperature	T_A	–	–40 to 85	°C
Storage temperature	T_{STG}	–	–65 to 150	°C

3.2 Recommended working conditions

The device needs to work under the recommended operating conditions. The electrical characteristic parameters listed in this chapter need to be guaranteed under the recommended conditions. The device's working conditions beyond the recommended conditions may reduce its reliability and even cause damage to the device.

Table 3-2 Recommended working conditions

Parameter	Symbol	Condition	Value	Unit
Operating Voltage	V_{DD}	–	1.8 to 5.5	V
Working temperature	T_A	–	–40 to 85	°C

3.3 I/O Port characteristics

Table 3-3 I/O Port characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Input high voltage	V_{IH0}	All ports, non-TTL mode V_{DD} = 1.8V to 5.5V	0.7 V_{DD}	–	V_{DD}	V
	V_{IH1}	TTL1 mode (PA0.0, PA0.1, PA0.3, PA0.4, PA0.6, PA0.7, PA0.13~PA0.15, PB0.0, PB0.2) V_{DD} = 5.0V	1.7	–	VDD	V
		TTL1 mode (PA0.0, PA0.1, PA0.3, PA0.4, PA0.6, PA0.7, PA0.13~PA0.15, PB0.0, PB0.2) V_{DD} = 3.0V	1.2	–	VDD	V
	V_{IH2}	TTL2 mode (PA0.6, PA0.7, PA0.13~PA0.15, PB0.0) V_{DD} = 5.0V	1.0	–	VDD	V
		TTL2 mode (PA0.6, PA0.7, PA0.13~PA0.15, PB0.0) V_{DD} = 3.0V	0.8	–	VDD	V
Input low voltage	V_{IL0}	All ports, non-TTL mode V_{DD} = 1.8V to 5.5V	–	–	0.3 V_{DD}	V
	V_{IL1}	TTL1 mode (PA0.0, PA0.1, PA0.3, PA0.4, PA0.6, PA0.7, PA0.13~PA0.15, PB0.0, PB0.2) V_{DD} = 5.0V	–	–	1.3	V
		TTL1 mode (PA0.0, PA0.1, PA0.3, PA0.4, PA0.6, PA0.7, PA0.13~PA0.15, PB0.0, PB0.2) V_{DD} = 3.0V	–	–	0.8	V
	V_{IL2}	TTL2 mode (PA0.6, PA0.7, PA0.13~PA0.15, PB0.0) V_{DD} = 5.0V	–	–	0.95	V
		TTL2 mode (PA0.6, PA0.7, PA0.13~PA0.15, PB0.0) V_{DD} = 3.0V	–	–	0.75	V
Output high voltage	V_{OH}	I_{OH} = -15mA, V_{DD} = 5V	V_{DD} – 1.0	–	–	V
Low output	V_{OL}	I_{OL1} = 15mA , V_{DD} = 5V	–	–	1	V

voltage		(All ports)				
	V_{OL2}	I_{OL2} = 120mA , V_{DD} = 5V (PB0.2, PB0.3, PA0.8, PA0.9 Strong pull-down drive mode)	–	–	1	V
High input leakage current	I_{LIH}	All ports, V_{IN} = V_{DD}	–	–	1	uA
Low input leakage current	I_{LIL}	All ports, V_{IN} = 0	–	–	–1	uA
Pull-up resistor	R_{PU}	V_{DD} = 5V, V_{IN} = 0V	25	50	75	kΩ
Pull-down resistor	R_{PD}	V_{DD} = 5V, V_{IN} = 5V	25	50	75	kΩ

I/O Port AC characteristics

Table 3-4 I/O Port AC characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Input the maximum frequency	IOF_{IN}	All ports		10		MHz
Output the maximum frequency	IOF_{OUT}	All ports		10		MHZ

3.4 Input reset characteristics

Table 3-5 Input reset characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Minimum low voltage pulse width	T_{NRST}	-	100	300	500	nS
nRESET Hysteresis voltage	V_{hyst}	Rise and fall		1		V

NOTE: The filter width of the input reset signal is 100 ns to 500 ns.
If the width of the input reset signal is less than 100ns, it will be regarded as an invalid signal (not reset).
If the width of the input reset signal is higher than 500ns, it will be regarded as a valid signal (reset)

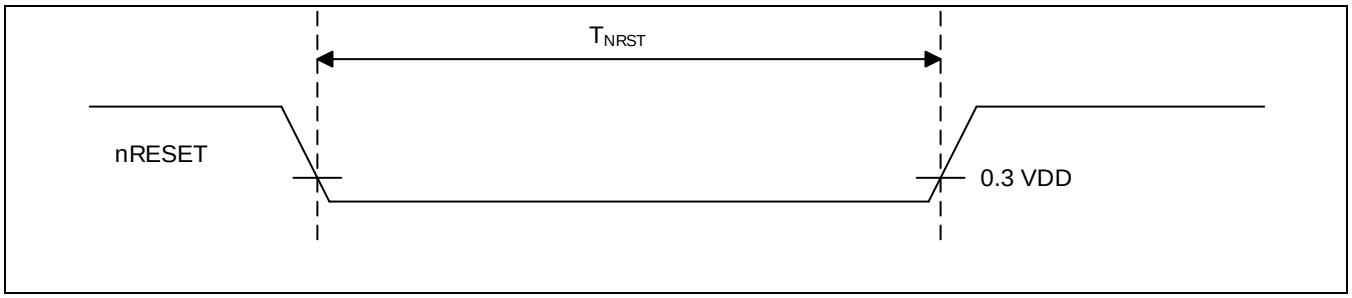


Figure 3-1 nRESET Input timing

3.5 Power-on reset characteristics

Table 3-6 Power-on reset characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Power-on power change rate	SR_{VDD}	-	0.1	-	-	V/mS

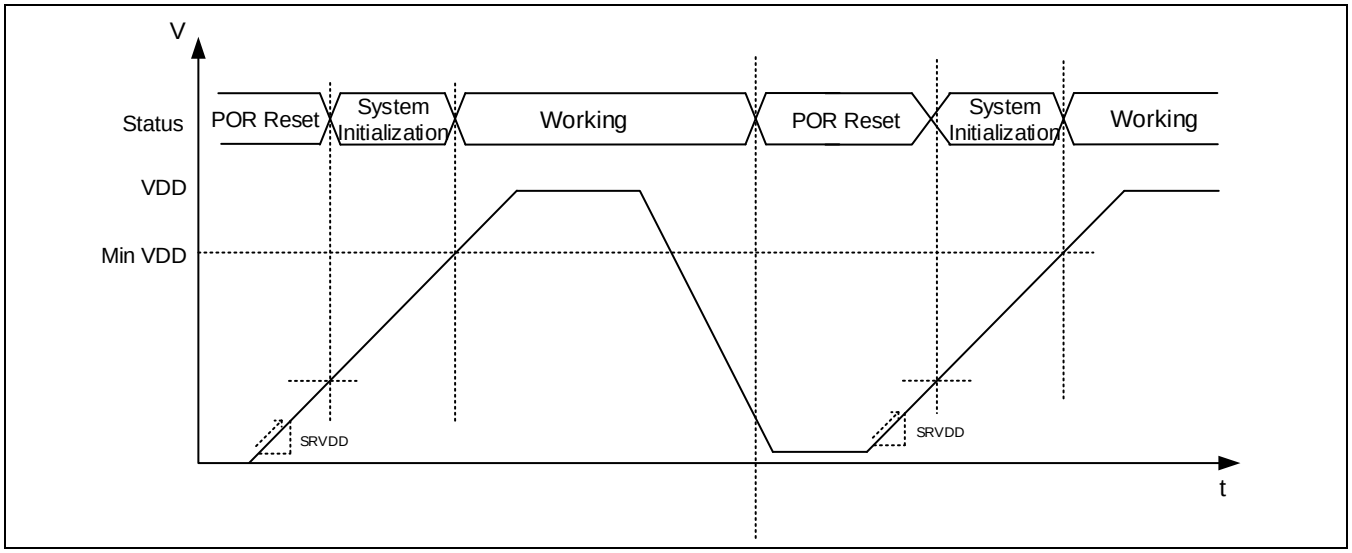


Figure 3-2 Schematic diagram of power-on and power-down

3.6 External interrupt input characteristics

Table 3-7 External interrupt input characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Interrupt input high pulse width	t_{INTH}	V_{DD} = 5.0V	15	30	45	nS
Interrupt input low pulse width	t_{INTL}	V_{DD} = 5.0V	15	30	45	nS

NOTE: The filter width of the input reset signal is 15 ns to 45 ns.
If the width of the input reset signal is less than 15ns, it will be regarded as an invalid signal.
If the width of the input reset signal is higher than 45ns, it will be regarded as a valid signal.

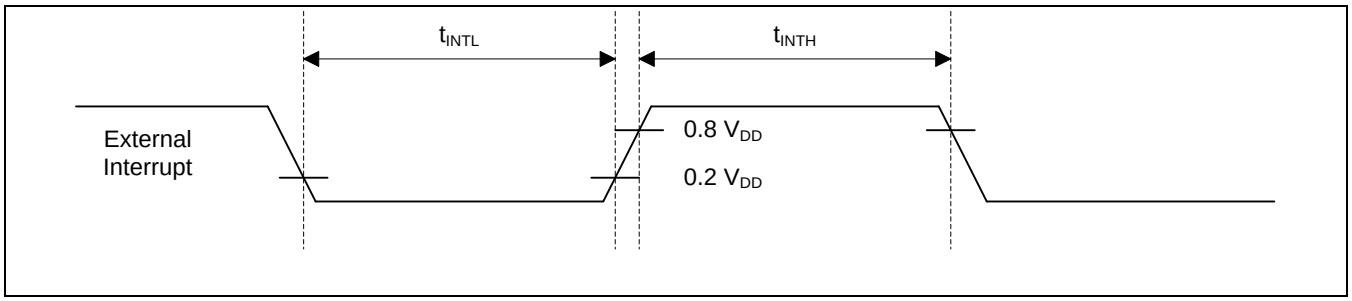


Figure 3-3 External interrupt input timing

3.7 Oscillator characteristics

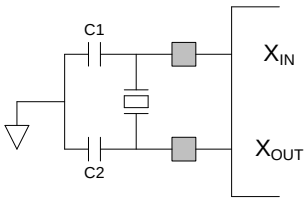
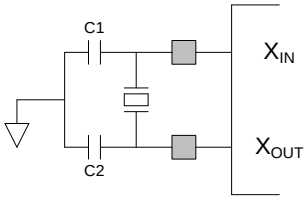
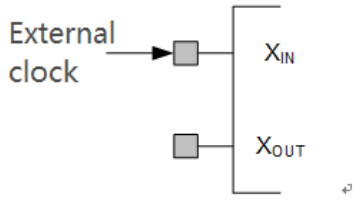
Three types of oscillators are included in the system:

- External main oscillator
- Internal main oscillator
- Internal sub-oscillator

3.7.1 External main oscillator

Table 3-8 External main oscillator characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Oscillator frequency	F_{EMOSC}	-	0.4	-	24	Mhz
Internal feedback resistance	R_{FD}	XIN Port	2	4	10	MΩ
stable schedule	T_{STA}	–	–	20	-	ms
External crystal oscillator (normal mode)	–		0.4	–	24	MHz
External crystal oscillator (low frequency mode)	–			32.768		KHz
External clock	–		0.4	–	24	MHz

3.7.2 Internal main oscillator characteristics

Table 3-9 Internal main oscillator characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Oscillator frequency	F_{IMOSC}	Mode1	-	5.556	-	MHz
		Mode2	-	4.194	-	MHz
		Mode3	-	2.097	-	
		Mode4	-	131.072	-	KHz
Duty cycle	T_{OD}	-	40	-	60	%
Accuracy after calibration	T_{ACC}	T_A = 25°C	-	-	±1	%
		T_A = –40 to 85°C	-	-	±3	%
Stable schedule	T_{STA}	After the power supply voltage reaches the minimum operating value	–	–	10	Clk

3.7.3 Internal high-speed oscillator characteristics

Table 3-10 Internal high-speed oscillator characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Oscillator frequency	F_{HFOSC}	Mode1	-	24	-	Mhz
		Mode 2	-	48	-	Mhz
Duty cycle	T_{OD}	-	40	-	60	%
Accuracy after calibration	T_{ACC}	T_A = 25°C	-	-	±1	%
		T_A = –40 to 85°C	-	-	±3	%
Stable schedule	T_{STA}	After the power supply voltage reaches the minimum operating value	–	–	10	Clk

3.7.4 Internal sub-oscillator characteristics

Table 3-11 Internal sub-oscillator characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Oscillator frequency	F_{ISOSC}	-	-	27	-	KHz
Duty cycle	T_{OD}	-	40	-	60	%
Precision	T_{ACC}	T_A = 25°C	-	-	±1	%
		T_A = –40 to 85°C	-	-	±5	%
Stable schedule	T_{STA}	After the power supply voltage reaches the minimum operating value	–	–	10	Clk

3.8 Working current

Table 3-12 Working current

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Description	Condition	State name	Minimum value	Typical value	Maximum value	Unit
Working current	I_{DD1}	normal work	V_{DD} = 5.0V , T_A = 25°C SYSCLK = 48MHz	RUN	–	3.6	–	mA
			V_{DD} = 5.0V , T_A = 25°C SYSCLK = 24MHz		–	2.5	–	
			V_{DD} = 5.0V , T_A = 25°C SYSCLK = 5.556MHz		–	0.8	–	
			V_{DD} = 5.0V , T_A = 25°C SYSCLK = 131KHz		–	0.45	–	
			V_{DD} = 5.0V , T_A = 25°C SYSCLK = 131KHz Enable Low Power Mode (SYSCON_OPT1:EFL_LPMD= 1)		–	0.25	–	
	I_{DD2}	CPU Clock off	V_{DD} = 5.0V , T_A = 25°C SYSCLK = 48MHz	SLEEP	–	1.0	–	mA
			V_{DD} = 5.0V , T_A = 25°C SYSCLK = 24MHz		–	0.7	–	
			V_{DD} = 5.0V , T_A = 25°C SYSCLK = 5.556MHz		–	0.18	–	
			V_{DD} = 5.0V , T_A = 25°C SYSCLK = 131KHz		–	0.10	–	
	I_{DD30}	All clocks and analog modules are closed	V_{DD} = 5.0V , T_A = 25°C	DEEP SLEEP	–	10	TBD	uA
			V_{DD} = 1.8V to 5.5V , T_A = –40 to 85°C		–	TBD	TBD	
	I_{DD31}	RTC uses 32KHz EMOSC to work, all clocks and analog modules except RTC are closed	V_{DD} = 5.0V , T_A = 25°C	DEEP SLEEP with RTC	–	33	TBD	uA
			V_{DD} = 3.0V , T_A = 25°C		–	21	TBD	
			V_{DD} = 1.8V to 5.5V , T_A = –40 to 85°C		–	TBD	TBD	
	I_{DD32}	RTC uses 27KHz ISOSC to work, all	V_{DD} = 3.0V ~ 5.0V , T_A = 25°C	DEEP SLEEP with RTC	–	12	TBD	uA
			V_{DD} = 1.8V to 5.5V ,		–	TBD	TBD	

Parameter	Symbol	Description	Condition	State name	Minimum value	Typical value	Maximum value	Unit
		clocks and analog modules except RTC are closed	T_A = –40 to 85°C					

NOTE: The operating current does not include the pull-up and pull-down current of the I/O port.

3.9 Low-voltage reset monitoring characteristics

Table 3-13 Low-voltage reset monitoring characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Low voltage reset voltage (VDD falling edge)	Vthrf	–	1.8	1.9	2.0	5V
		–	2.1	2.2	2.3	
		–	2.4	2.5	2.6	
		–	2.7	2.8	2.9	
		–	2.95	3.1	3.25	
		–	3.25	3.4	3.55	
		–	3.55	3.7	3.85	
		–	3.85	4.0	4.15	
Low voltage monitoring voltage (VDD falling edge)	Vthdf	–	2.0	2.1	2.2	
		–	2.3	2.4	2.5	
		–	2.6	2.7	2.8	
		–	2.85	3.0	3.15	
		–	3.15	3.3	3.45	
		–	3.45	3.6	3.75	
		–	3.75	3.9	4.05	
Hysteresis voltage	ΔV_{LVD}	–	–	200	–	mV
Working current	I_{CC}	–	–	9	–	uA
Shutdown current	I_{PD}	–	–	0.1	–	uA

3.10 12 Bit A/D converter characteristics

Table 3-14 12 Bit A/D converter characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Precision	–	–	–	12	–	Bit
Operating Voltage	V_{ADC}	–	1.8(1)	5	5.5	V
Reference reference voltage	V_{REF}	V_{REF} <V_{ADC}	2	5	5.5	V
Input voltage range	V_{AIN}	–	0	–	V_{REF}	V
Conversion rate	F_S	–	–	–	1	MHz
Differential nonlinearity	DNL	F_S = 0.5MHz V_{ADC} = 5V	–	-	±2.0	LSB
Integral nonlinearity	INL		–	-	±4.0	
Offset error	TOPOFF		–	-	±10.0	
	BOTOFF		–	-	±10.0	
Working current	I_{OP}	–	–	1	–	mA
Shutdown current	I_{PD}	–	–	1	–	μA
ADC clock frequency	F_{ADC}	–			24	MHz
ADC conversion period	T_{conv}	T_{sample} = 8		24		T_{ADC}
External input impedance	R_{AIN}	F_{ADC} = 1MHz V_{ADC} = 5V T_{sample} = 8			150(2)	K

NOTE: The above data are application evaluation results, not mass production test results.

(1) ADC speed is limited when working under low voltage. When working at 1.8V, the ADC clock frequency should be less than 500KHz.

(2) The input impedance of the ADC is related to the working clock frequency of the ADC and the number of sampling cycles. CADC is the internal sample and hold capacitor, and the charging time of this capacitor needs to meet TC=10 x (RADC+RAIN) x CADC. Among them, RDAC is the sampling switch resistance, the maximum value is 1K; CADC is the internal sampling and holding capacitor, the maximum value is 5pF.

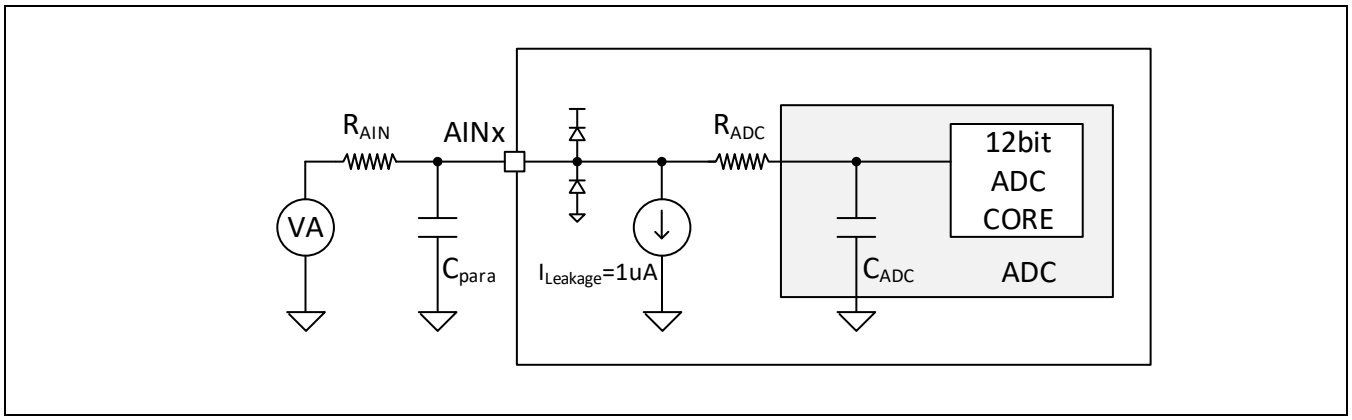


Figure 3-4 ADC Sample connection diagram

3.11 Internal fixed reference voltage characteristics

Table 3-15 Internal fixed reference voltage characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Low reference voltage	FVR_L	-	-	2.048	-	V
High reference voltage	FVR_H	-	-	4.096	-	V
Low reference voltage accuracy	Vaccl	V_{DD} = 5.0V T_A = 25°C	-	-	1%	-
		V_{DD} > 2.7V T_A = –40 to 85°C	-	-	2%	-
High reference voltage accuracy	Vacch	V_{DD} = 5V T_A = 25°C	-	-	1%	-
		V_{DD} = 5V T_A = –40 to 85°C	-	-	2%	-

3.12 Internal INTVREF reference voltage characteristics

Table 3-16 Internal INTVREF reference voltage characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
INTVREF Reference voltage	$V_{INTVREF}$	-	-	1.0	-	V
INTVREF Precision	Vacc	T_A = 25°C	-	-	1%	V
		T_A = –40 to 85°C	-	-	2%	V

3.13 Memory characteristics

Table 3-17 RAM和Register characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Data retention voltage (1)	V_{DDDR}	Deep sleep mode	0.8	–	V_{DD}	V

NOTE: 1）The lowest voltage value to ensure that the data in the RAM is not lost (in deep sleep mode), or the lowest voltage value to maintain the state of the register (in deep sleep mode). Guaranteed by design, not tested in mass production.

Table 3-18 FLASH Characteristics of memory

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Programming size	F_{WSIZE}	–	–	4	–	Byte
Page size	$F_{PROMSIZE}$	–	–	256	–	Byte
	$F_{DROMSIZE}$			64		Byte
Programming time (1Word)	F_{tprog}	–	20	–	–	us
Page erase time	F_{tpera}	–	2	–	–	ms
Full chip erasing time	F_{tmera}	–	10	–	–	ms
Programming times	F_{nwe}	–	100,000	–	–	Times
Data retention time	F_{tdr}	–	10	–	–	Years
Power consumption (when programming or erasing)	F_{idd}	–	–	–	5	mA

3.14 Electrostatic protection (ESD) characteristics

Table 3-18 Electrostatic protection characteristics

Parameter	Symbol	model	Minimum value	Typical value	Maximum value	Unit
Static protection withstand voltage	V_{ESD}	HBM	4000	–	–	V
		MM	200	–	–	V
		CDM	500	–	–	V

4 Package size

4.1 APT32F1023 Support package type

SSOP24

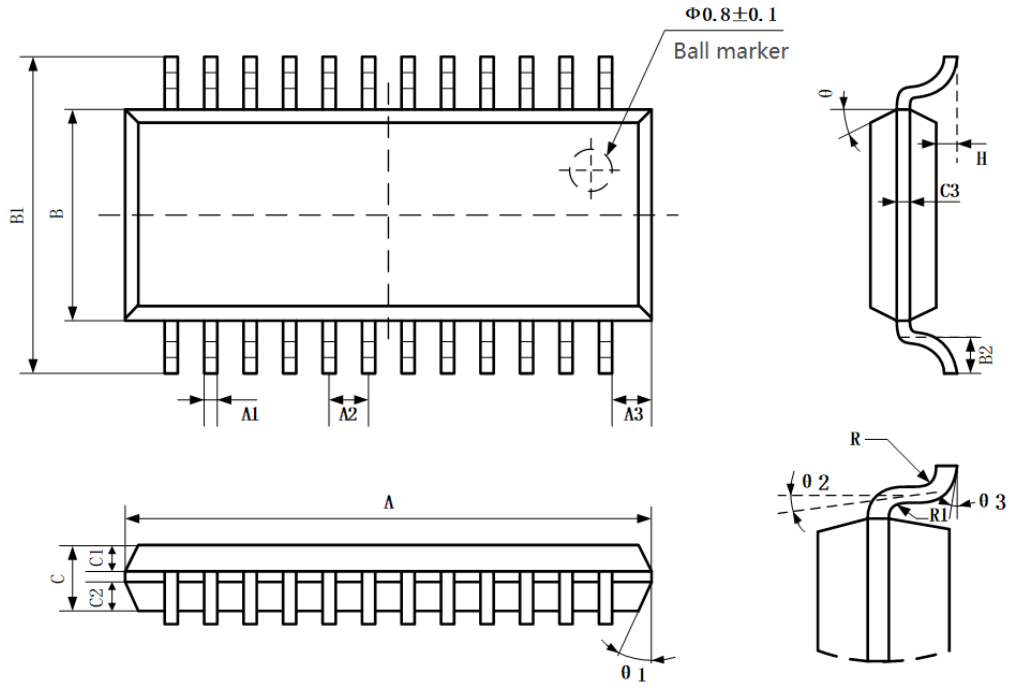
SOP24

SOP20

QFN20

SOP16

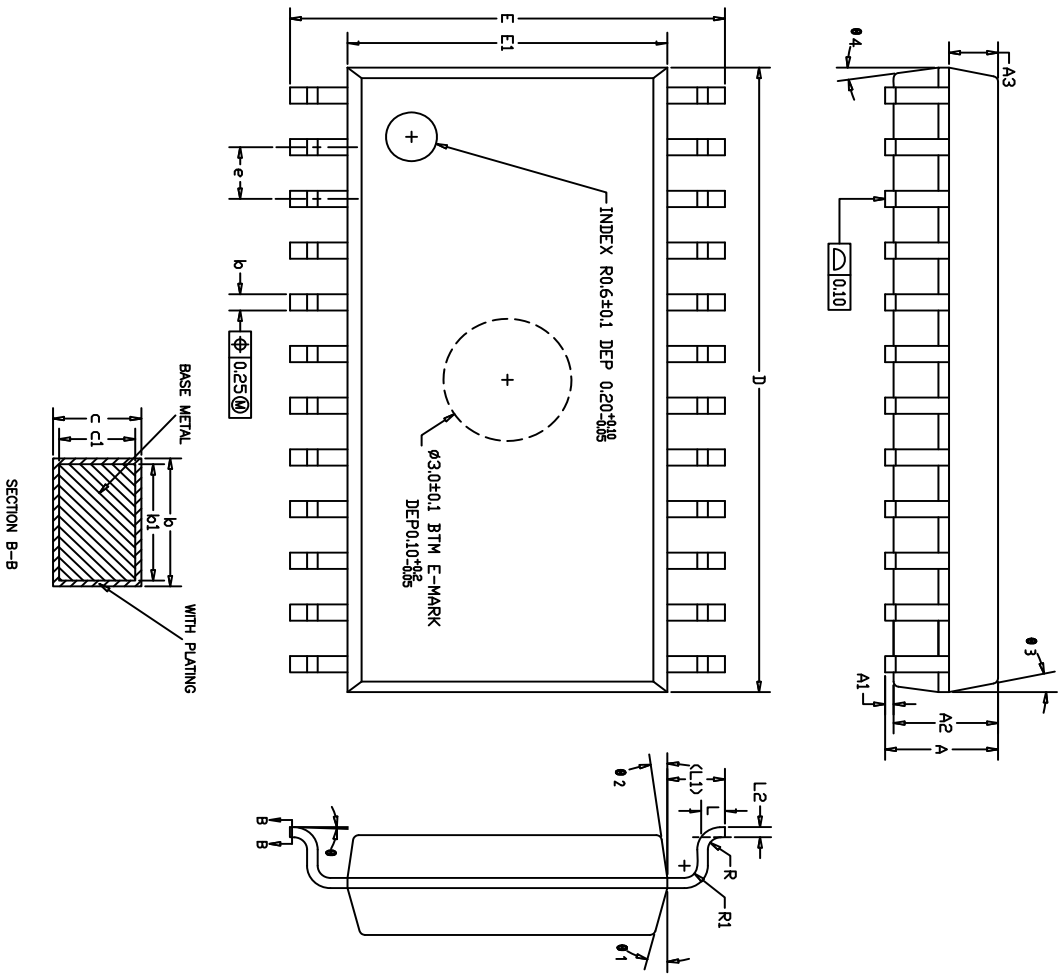
4.2 SSOP24



Symbol / Size	Min(mm)	Max(mm)	Symbol / Size	Min(mm)	Max(mm)
A	8.60	8.70	C3	0.203TYP	
A1	0.254 TYP		H	0.1	0.25
A2	0.635 TYP		θ	8° TYP	
A3	0.705 TYP		θ1	7° TYP	
B	3.85	3.96	θ2	4° ~ 12°	
B1	5.80	6.20	θ3	0° ~ 8°	
B2	0.40	0.70	R	0.20 TYP	
C	1.40	1.50	R1	0.20 TYP	
C1	0.40	0.70			
C2	0.55	0.65			

Figure 4-1 SSOP24 (0.635mm) Package size

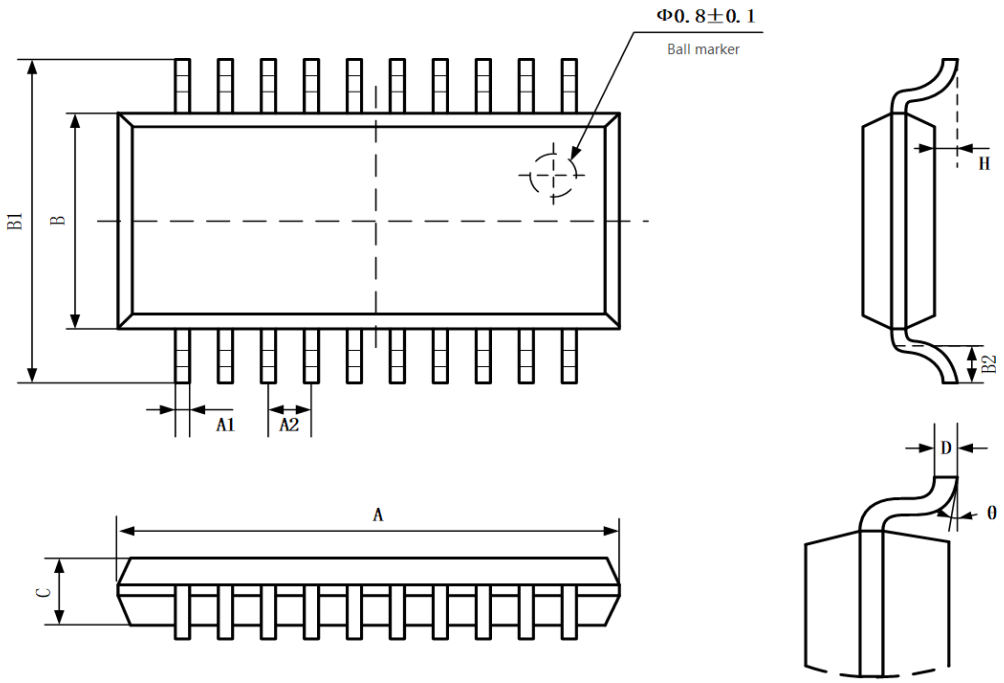
4.3 SOP24



SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	2.35	2.60	2.80	e		1.27BSC	
A1	0.05	0.15	0.30	L	0.40	0.60	0.80
A2	2.25	2.45	2.65	L1		1.35REF	
A3	1.05	1.15	1.25	L2		0.25BSC	
b	0.36	–	0.49	R	0.10	–	–
b1	0.35	0.40	0.45	R1	0.10	–	–
c	0.21	–	0.34	θ	0°	–	8°
c1	0.20	0.25	0.30	θ1	13°	15°	17°
D	15.24	15.34	15.44	θ2	6°	8°	10°
E	9.80	10.20	10.60	θ3	9.5°	11.5°	13.5°
E1	7.40	7.50	7.60	θ4	6°	8°	10°

Figure 4-2 SOP24 (1.27mm) Package size

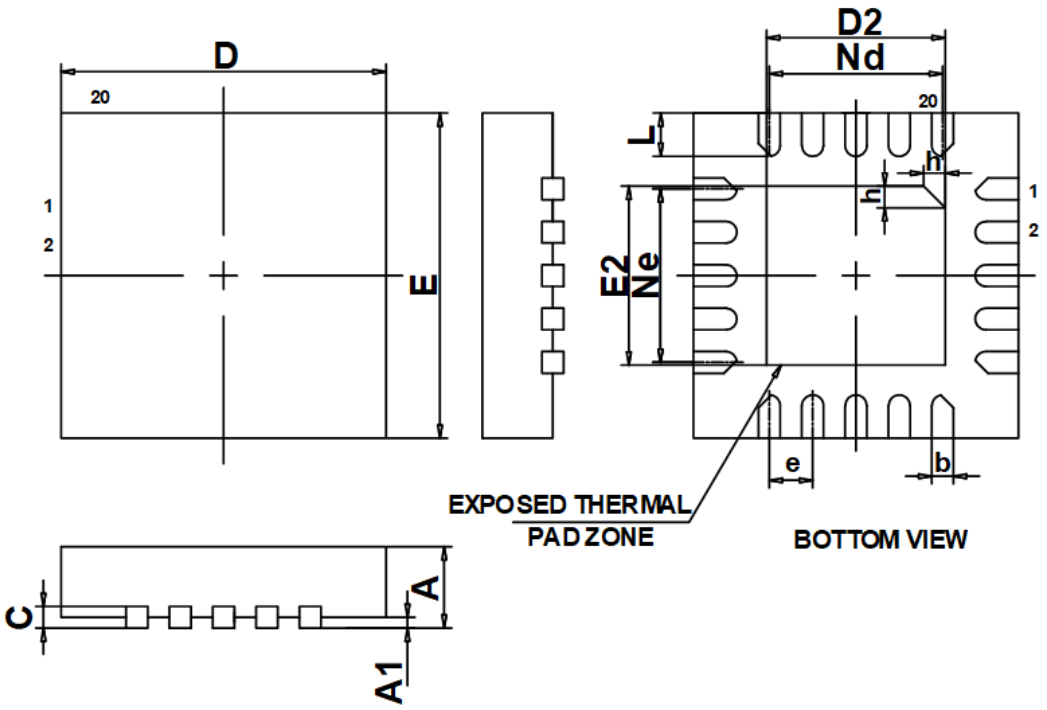
4.4 SOP20



Symbol / Size	Min(mm)	Max(mm)	Symbol / Size	Min(mm)	Max(mm)
A	12.40	13.00	H	0.05	0.25
A1	0.40 TYP		θ	8° TYP	
A2	1.27 TYP				
B	7.40	7.90			
B1	10.15	10.45			
B2	0.60	1.00			
C	2.15	2.55			
D	0.25 TYP				

Figure 4-3 SOP20 (1.27mm) Package size

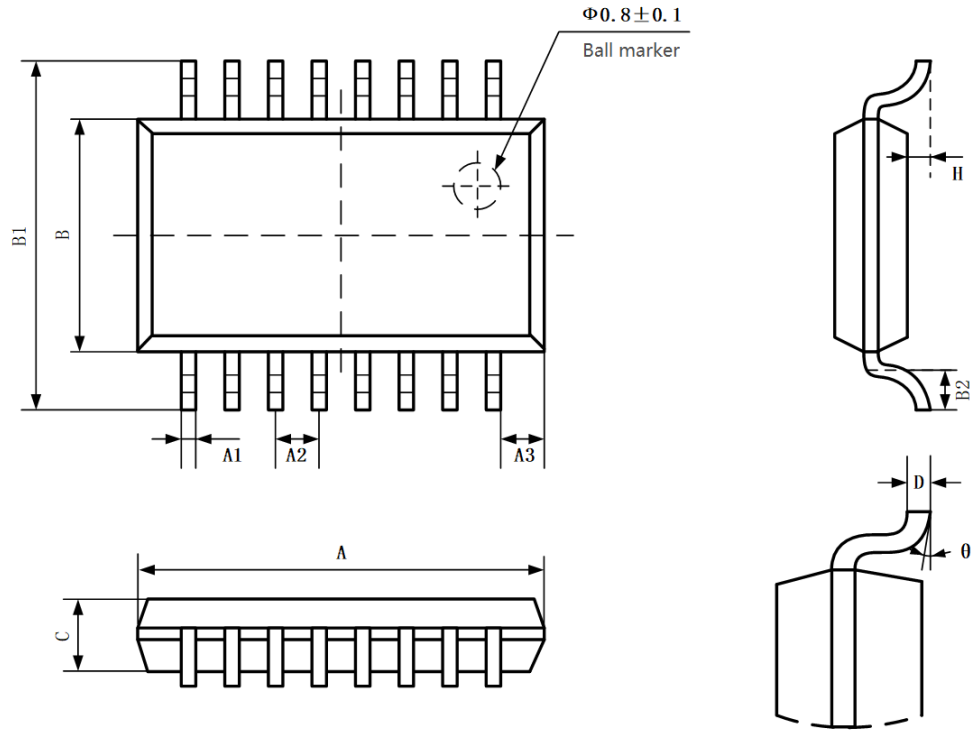
4.5 QFN20



Symbol / Size	Min(mm)	Nom(mm)	Max(mm)	Symbol / Size	Min(mm)	Nom(mm)	Max(mm)
A	0.70	0.75	0.80	E2	1.55	1.65	1.75
A1	-	0.02	0.05	L	0.35	0.4	0.45
b	0.15	0.20	0.25	h	0.2	0.25	0.3
c	0.18	0.20	0.25	L/F(mil)	75*75		
D	2.90	3.00	3.10				
D2	1.55	1.65	1.75				
e	0.40 BSC						
Ne	1.60 BSC						
Nd	1.60 BSC						
E	2.90	3.00	3.10				

Figure 4-4 QFN20 (0.40mm) Package size

4.6 SOP16



Symbol / Size	Min(mm)	Max(mm)	Symbol / Size	Min(mm)	Max(mm)
A	9.80	10.00	H	0.1	0.25
A1	0.45 TYP		θ	8° TYP	
A2	1.27 TYP				
B	3.70	4.10			
B1	5.80	6.20			
B2	0.35	0.65			
C	1.30	1.50			
D	0.25 TYP				

Figure 4-5 SOP16 (1.27mm) Package size

5 Ordering Information

5.1 Product naming convention

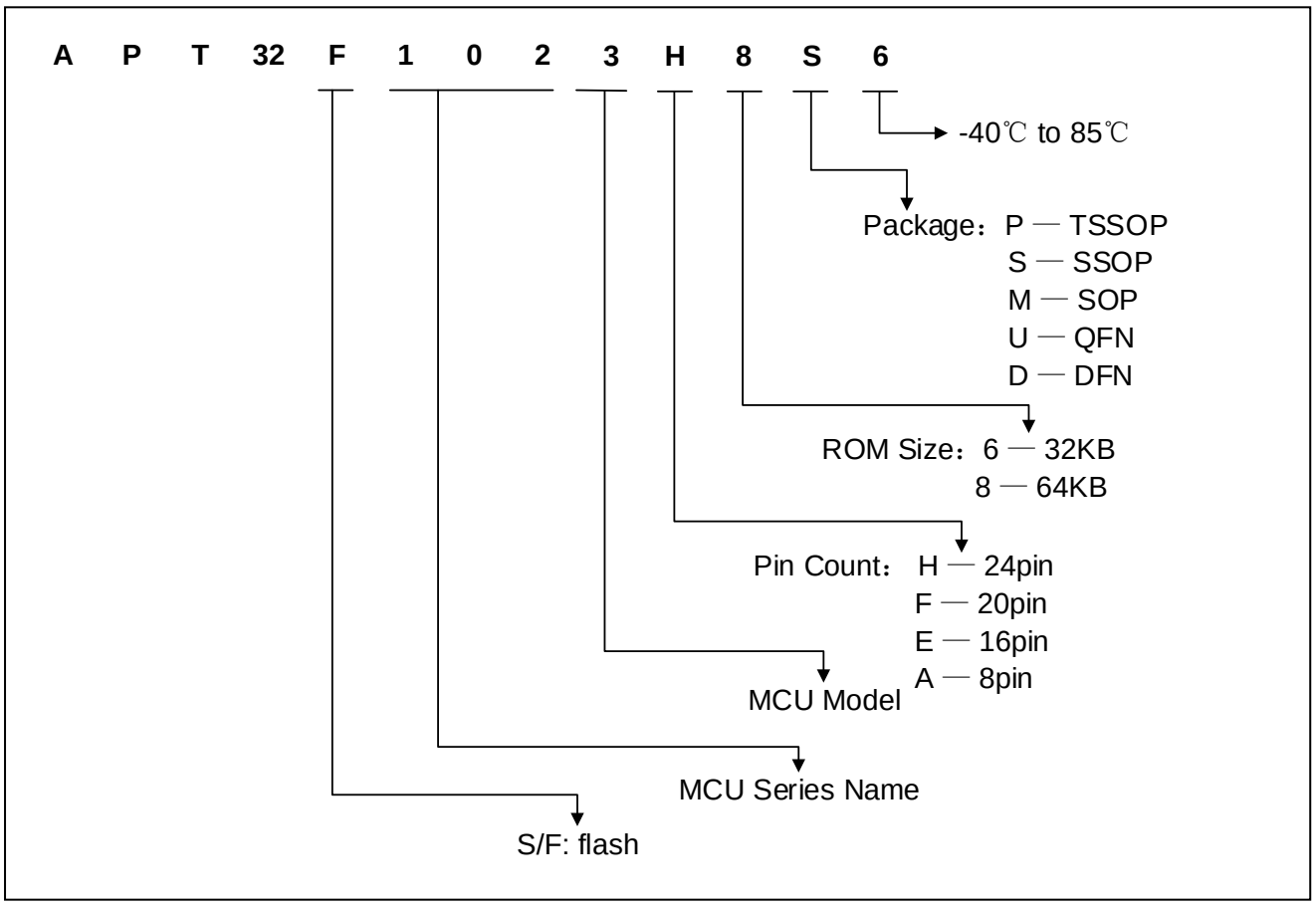


Figure 5-1 Product naming convention

5.2 Series product order model

Table 5-1 APT32F1023 Product order model description

Series	Model details
1023	APT32F1023H8S6/APT32F1023H6S6 APT32F1023H8M6/APT32F1023H6M6 APT32F1023F8M6/APT32F1023F6M6 APT32F1023F8U6/APT32F1023F6U6 APT32F1023E8M6/APT32F1023E6M6